RADIATION SENSITIVITY OF SPICE MODEL PARAMETERS OF MOSIS CMOS DEVICES

A Thesis

Submitted to the Graduate Faculty of the
Louisiana State University and
Agricultural and Mechanical College
in partial fulfillment of the
requirements for the degree of

Master of Science in Electrical Engineering

in

The Department of Electrical Engineering

by
Roy Austin Hensley
B.S. in E.E., Louisiana State University, 1991
May 1993

ACKNOWLEDGMENTS

The author would like to express his gratitude to the many who have helped him during the course of this thesis: Dr. Ashok Srivastava for his guidance and patience, Dr. Pradeep Bhattacharya and Dr. John Courtney for enlightening discussions, the Nuclear Science Center for providing graphic services and supplies, Dr. Martin Feldman for generously offering use of his palladium X-ray source, Golden Hwaung and Sunil Andhole for their assistance in performing X-ray exposures, Dr. Pratul Ajmera for providing access to the Solid State Laboratory and for allowing use of the new probing station, Dr. Kiki Ikossi-Anastasiou for permitting use of and for configuring the HP I-V measurement system, Steve Schmeckpeper for repairing the HP 4140B, and Susan Dodson for proof-reading this work and for her companionship. I am greatly indebted to all of you.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

The effects of radiation upon CMOS circuits and devices are a major concern in their use in harsh environments. In this thesis, SPICE model parameters were extracted as functions of dose from devices fabricated by the MOSIS two micron technology. It was shown that this process imparts radiation-hardened properties. Further, these properties were exploited in a modified CMOS static memory cell design that compensates for threshold voltage shift in n-channel transistors.

CHAPTER 1

INTRODUCTION

Damage to electronic materials by ionizing radiation is a topic of interest to many, from the military to the semiconductor industry. In either case, the bottom line is the degree of a circuit's or a device's survivability in harsh environments such as space. Metal Oxide Semiconductor (MOS) devices, the foundation of Complimentary MOS (CMOS) technology, typically exhibit shifts in threshold voltage, decreased carrier mobility, and increased leakage currents when exposed to ionizing radiation. These changes tend to degrade circuit performance and function.

Though CMOS devices have been in commercial use for only thirty years, the study of ionizing radiation's effects on matter has a long history. X rays were discovered in 1895 by Roentgen and are composed of photons, which are massless, neutral particles. Gamma rays share this composition but are emitted by nuclei and are generally of higher energy than X rays. The resulting effect of an interaction between one of these rays and an atom is usually one of ionization. It is a conceptually simple but calculably complicated multimodal process.

Three basic types of interaction may be defined where the probability of each is a function of the photon energy and the associated energy state and type of the atom. Each

of these are illustrated in Figure 1.1. Appearing first is pair production. In this process, the incident photon is completely absorbed and an electron-positron pair is created in its place. Pair production is induced by the strong electric field that exists close to the nucleus; it has a threshold energy of $2m_ec^2$, or 1.02 MeV. The second interaction type is Compton scattering and is dominant at intermediate energies. Stated simply, a photon of energy E interacts with an electron initially at rest. The electron is freed from the atom and has kinetic energy KE while the incident photon donates energy and is scattered with a resulting energy of E' = E - KE - binding energy. If the energy of the resulting photon is high enough, it can in turn ionize other atoms in the lattice, as can the freed electron through collision if its kinetic energy is high enough.

The third and final interaction type is the photoelectric effect. This effect demands special attention as it is the dominant interaction for lower energy photons (see Figure 1.2 [1]). In the photoelectric effect, a photon interacts with the entire atom. Resulting is the emission of a photoelectron, usually from the K shell of the atom, leaving a hole behind. Momentum is conserved by the recoil of the target atom. The photon energy in excess of the electron binding energy Eb is divided inversely with the masses of the electron and the atom. Therefore, for the higher Z materials, we may assume KE ≈ E - Eb for the

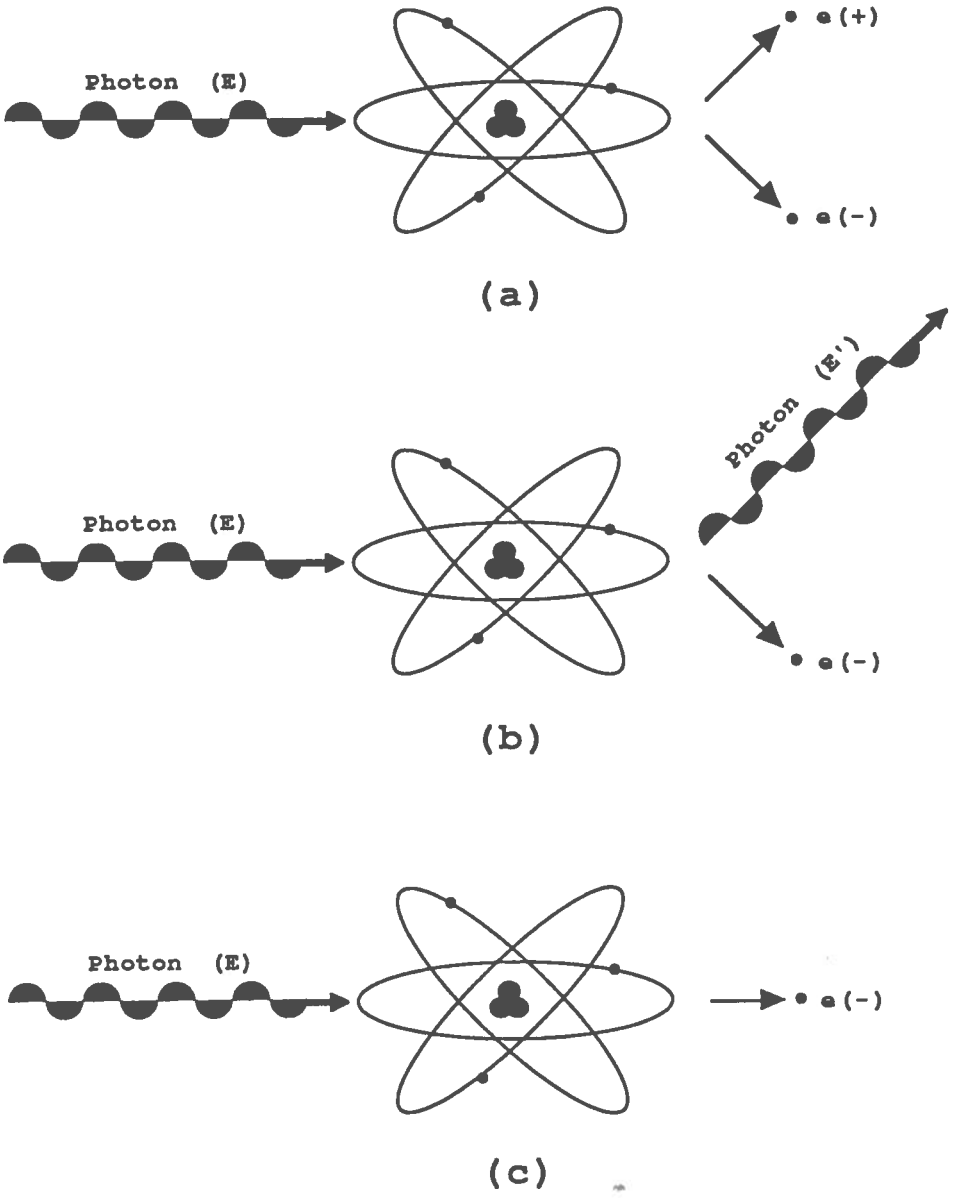


Figure 1.1. Photon interactions with matter.
(a) Pair production
(b) Compton effect
(c) Photoelectric effect

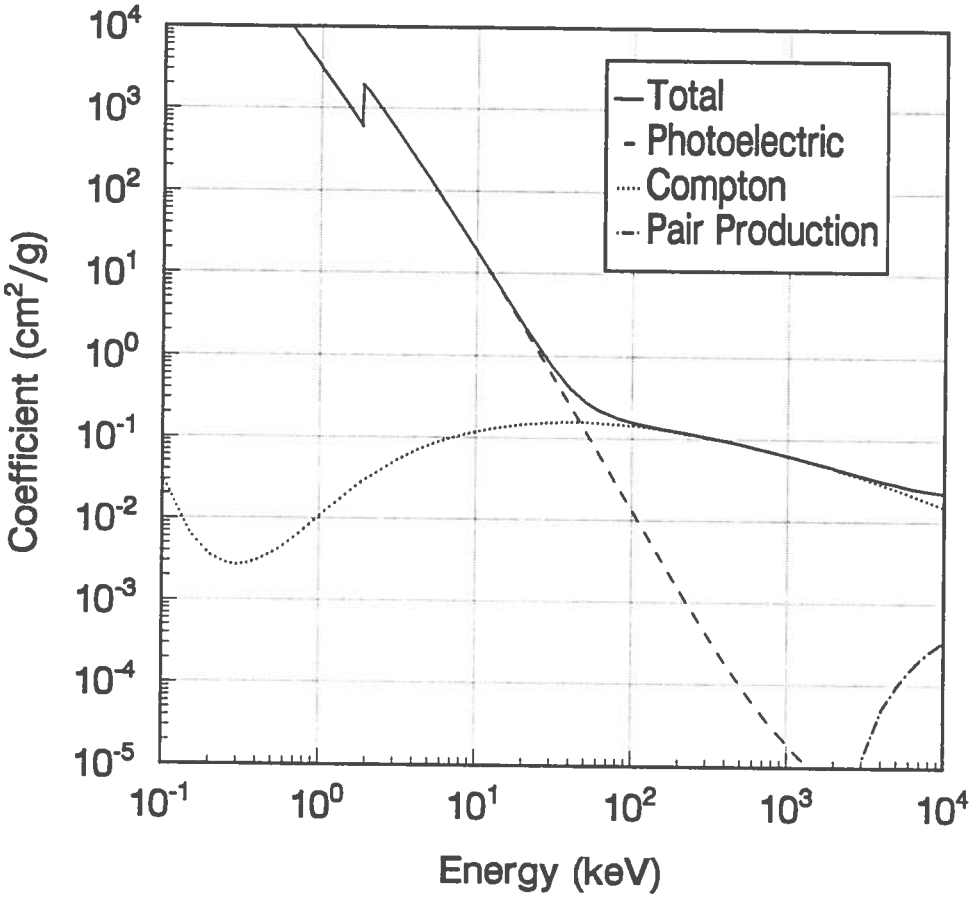


Figure 1.2. Mass attenuation coefficients for various photon interactions in SiO_2

photoelectron. K shell binding energies range from 13.6 eV for hydrogen to 116 keV for uranium [2]. As a rule of thumb, about eighty percent of photoelectric interactions with heavy nuclei result in the ejection of a K shell electron, while K shell electrons are responsible for essentially all photoelectric interactions with light nuclei [2].

Referring once more to Figure 1.2, an interesting note may be made. As the photon energy decreases, the probability of photoelectric interaction increases until the photon energy becomes equal to a K shell energy. At this point, the probability drops discontinuously. This illustrates the idea of a "K edge" [2]. As the photon energy decreases further, the probability increases once again until the first L edge is reached. The probability of photoelectric interaction drops as before, then builds up until the next L edge is encountered, and so on.

The net result is an abundance of free electrons in the material lattice during irradiation as well as a slight increase in the thermal energy of the material lattice. The former is generally of greater significance to the welfare of a semiconductor device than the latter. A device's type as well as the materials it is made of have a great impact on the extent of damage and the degree to which that damage may impair device functionality or reliability.

The primary ionization-induced changes in the bulk material are conductivity, which increases due to the production of excess charged carriers (electron-hole pairs), and trapped charges in the oxide insulator which result in the production of electric fields due to the separation of charges. In silicon, experiments reveal that about 3.6 eV is expended to create an electron-hole pair [3]. Generalizing a bit further, the electron-hole creation energy tends to be about two the 18 eV gap energy for semiconductors and insulators [3]. This may be a hundredth or even a thousandth of the energy typically associated with an X or gamma ray, which puts into perspective the magnitude of kinetic energy a charged particle may depart with to carry out subsequent ionizations. If an electron is freed only to not have enough energy to span the forbidden gap in an intrinsic material, it may still interact. In many cases dopants are present in the semiconductor and these form defect complex sites within the gap. The free charge carrier may have enough energy to span this shorter distance and become trapped there, producing a negative charge in the oxide or neutralizing a positive charge center.

Another fate of electrons may be their leaking to a surface. If this is the case, the material may be left with a net positive charge. Similarly, if electrons are captured in a material a net negative charge may result. Either of these events can give rise to the aforementioned creation of

an electric field which in turn creates a potential difference across the interface between the donating and accepting materials. A current then begins to flow across the interface in accordance with Ohm's law, tending to balance the effect.

A similar series of events exists in insulators, such as the gate oxide in a MOS Field Effect Transistor (FET). Charge carriers can escape from the oxide, creating an electric field in the oxide which is induced by charge separation. At the same time, conductivity is continually increased by the ionization process. If the increase is sufficient, a counter-current may be established which yields a saturation of the electric field. Once removed from the X- or gamma ray environment the carriers gradually drift back and recombine, some becoming trapped in the defect complex sites. It should be noted that the diffusion and conduction processes in insulators are modified by the fact that many important insulators are noncrystalline. Furthermore, traps are more numerous in insulators than in semiconductors and holes and electrons are usually captured at different sites [4].

The importance of oxide charges has been established and further explanation of those that are relevant is in order. Figure 1.3 shows the general types of oxide charges [5]. The $Si-SiO_2$ interface region is one of abrupt transition from crystalline Si to amorphous SiO_2. This results in dangling

bonds called interface states, or Q_{it} in Figure 1.3. At the surface of a freshly cleaved piece of semiconductor there are usually dangling valence bonds from the valence electron sites which are not paired with electrons as they are in the bulk. The discontinuity in the electron binding results in extra states for the electrons over and above those in the bulk. These are called surface states and can be divided into two groups: donor-like states, which are positively charged when they lie above the Fermi level, and acceptor-like states, which are negatively charged when they lie below the Fermi level.

Another difficulty arises from the fact that during thermal oxidation the substrate dopant diffuses through the interface and into the oxide which results in the formation of neutral hole and/or neutral electron traps. Finally, these traps may be filled by charge carriers, freed by ionizing radiation, to create the oxide-trapped charges, or Q_{ot} in the figure. A manifestation of this may be observed in positive charge buildup above substrates. The surface silicon can become partially depleted of electrons. With the introduction of parasitic leakage paths, two or more devices may become coupled, leading to circuit failure due to latchup [6].

Electrical contacts to insulators are important considerations in the irradiated insulator scenario as well. The Fermi level of a metal is generally far below the conduction

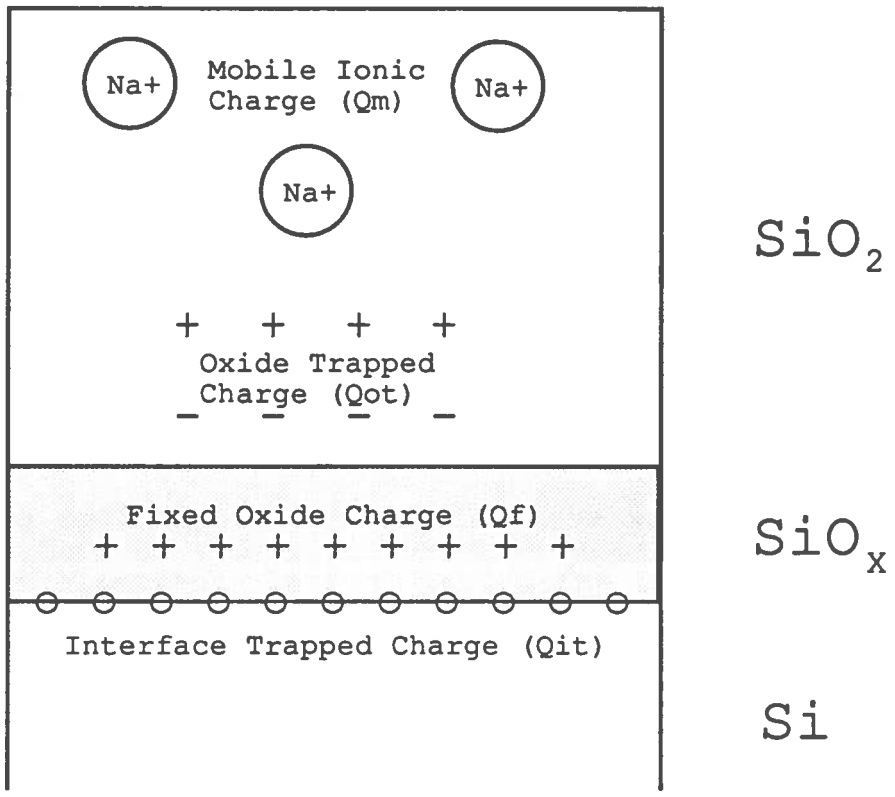


Figure 1.3. Charges in thermally oxidized silicon

level of an insulator at room temperature. This implies that the metal can readily accept electrons from the insulator but cannot donate electrons to it except under the influence of a high electric field, high temperature, or, of more immediate interest, charge transfer due to radiation [4]. The metal-to-insulator and semiconductor-to-insulator charge transfers are not always favored though. This may lead to a charge accumulation at one of these two interfaces which may have important device implications [4].

Perhaps the most obvious change in a device, NMOS and PMOS alike, is a shift in the threshold voltage, V_T. As previously discussed, electron-hole pairs are created by the ionizing radiation. The applied gate voltage depletes the oxide of electrons, leaving behind the lower mobility holes for a net positive charge in the oxide. If the gate voltage is positive, the holes travel toward the Si-SiO_2 interface and become trapped there, while a negative gate voltage will trap holes near the SiO_2-gate metal interface. These trapped positive charges tend to shift the threshold more negative for both n- and p-type transistors, as shown in Figure 1.4. The smaller the span of distance between the gate terminal and these charges and with other variables remaining constant, the less the effect the charges have on the threshold voltage. Following this reasoning, the PMOS transistor would be more radiation hard than the NMOS transistor.

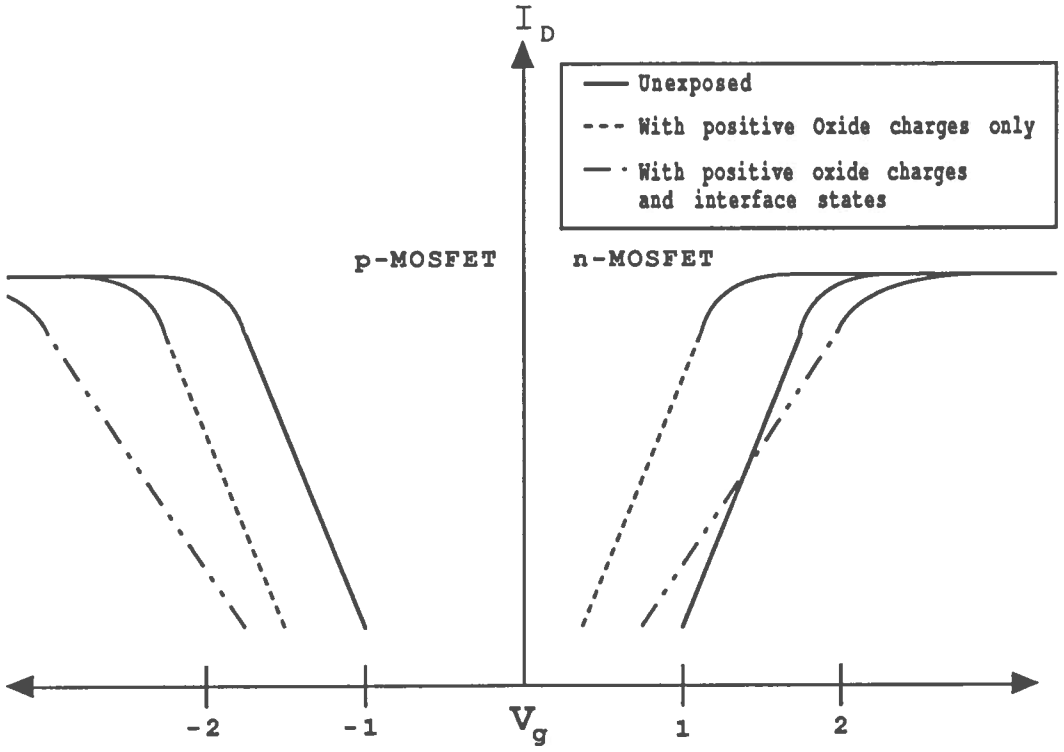


Figure 1.4. The effect of interface states and positive oxide charge on the shift and distortion of p- and n-channel MOSFET I-V

The negative shift of both threshold voltages is not the case for all doses, however. At high doses the threshold voltage of an n-channel device can actually become more positive. This rebound may be attributed to negative charges contributed by electrons trapped in acceptor-like interface states [7].

From a practical point of view however, the measurement of the X- and gamma ray-induced damage is just as important as the microscopic characterization of its effects on devices. Fortunately, many types of radiation induced damage can be measured at least indirectly. Some of the properties of semiconductors which are sensitive to and give information about the nature of radiation-induced defects are conductivity, the Hall coefficient, mobility, and breakdown voltage.

Though there are a number of techniques, perhaps the most frequently employed and powerful means of characterization is capacitance-voltage (CV) measurements. Some of the properties that can be quantified with this approach are flatband voltage, mobility, doping density, and fixed oxide charge. Alternatively, current-voltage (IV) measurements may be employed. This method is based upon very reliable analytical models which predict the relationships between currents and voltages in MOSFETs. Among the many parameters which may be determined are the threshold voltage and the carrier surface mobility, the most important to the digital

circuit designer. By studying these parameters as functions of dose, the relative radiation hardness of a particular device or circuit can be ascertained.

Unfortunately, the MOS devices on which the CMOS circuit technology is built are among the least resistive device types to radiation damage. CMOS is the preferred technology in modern integrated circuit design due to its low power consumption, density, and simplicity. Ironically, damage to conventional CMOS circuits can ultimately result in a tremendous increase in power dissipation leading to device failure.

The point at which circuit failure occurs depends on several factors, including the processing conditions under which the devices were fabricated and the actual design of the circuit. In other words, good processing can result in an inherent hardness to the effects of radiation, as can a good design. By modeling circuits using empirically determined radiation sensitive parameters, different processing technologies and design methodologies may be evaluated and improved.

One of the more popular device and circuit modeling tools is SPICE [8]. This general purpose circuit simulator was developed in the mid-1970's at the University of California, Berkeley. SPICE is an acronym that stands for Simulation Program with Integrated Circuit Emphasis.

Circuits may contain a myriad of devices including resistors, capacitors, inductors, programmable current and voltage sources, and the four most common semiconductor devices: diodes, BJTs, JFETs, and MOSFETs. The electronic devices are represented in the program by built-in mathematical models; variables in these models are often referred to as model parameters. These quantities allow tailoring of models to fit unique, real-world devices.

CHAPTER 2

REVIEW OF LITERATURE

Many issues regarding radiation damage to CMOS structures and the testing thereof have been addressed in research literature over the last thirty years. To date, there does not exist a general analytical model which can predict the behavior of a device affected by radiation over any reasonable cross-section of geometries and processing conditions. The large number of factors involved in determining the extent and type of damage that a device might incur has yielded results which are quantitatively applicable only to those devices which are designed, manufactured, and exposed exactly as the test subjects were. Fortunately, there has been sufficient agreement among the data to give a good qualitative understanding of radiation damage with regard to many of these variables.

Photon energy is a parameter whose influence on damage is debated, however. This is a significant consideration as the most popular radiation sources are X-ray machines and Cobalt-60 (^{60}Co). X ray energies are frequently below 10 keV while photon energies from ^{60}Co average 1.25 Mev. Clearly, different photon interactions are favored at each of these energies. Some research has shown an energy dependence [9,10], while other work has observed no effect [11]. From those investigations that observed an energy influence, there

is some indication of a process dependent factor as well as the number of interface states created being proportional to the incident photon energy. Aside from the physics of photon interactions, dosimetry for practical high energy gamma irradiation facilities is greatly complicated by Compton scattering both inside and around the source. The effect creates a softening of the gamma spectrum within the device compared to that incident on it. The mass attenuation coefficients used for calculating absorbed dose in a target vary significantly with photon energy. It is possible that a portion of the differing observations of energy dependence is a result of such an effect.

Dose rate dependency is another controversial topic. Many studies, usually employing both X-ray and ^{60}Co sources, claim that this has a significant impact on the resulting device damage [10,12,13]. Focus is generally placed on an increased number of interface states at the lower dose rates. Other researchers have shown that if the exposure is corrected for energy and the time between the beginning of exposure and the time of measurement, dose rate has no effect [14].

This observation sheds light on an important factor which influences the observed damage: annealing. The time and temperatures involved can affect the threshold voltage significantly by influencing the numbers of oxide-trapped and interface-trapped charges [12,13,15,16]. Additionally, bias

can have a significant effect on charge buildup and decline both during exposure and after. Recall that oxide-trapped charge tends to be positive, contributing to a negative shift in threshold voltage. Interface-trapped charge is not the same for both device types, however. It tends to be negative for n-channel devices, increasing the threshold voltage, and positive for p-channel devices, decreasing the threshold voltage.

The dynamics of these charges collectively shape the threshold voltage. After irradiation, V_T initially exhibits a positive shift with respect to time. This recovery is due, at least in part, to annealing of the oxide-trapped charge; interface-trapped charge does not tend to decrease. Under positive bias conditions during the anneal, interface-trapped charge may greatly increase in an NMOS transistor [16]. The resulting n-channel threshold voltage can reach a value in excess of the pre-irradiated value. This condition is often referred to as "super recovery" and is generally observed only at high doses where interface-trapped charge dominates oxide-trapped charge [17, p. 266]. Super recovery does not occur for PMOS devices, however. If it happens that interface-trapped charge increases in a p-channel transistor, the threshold voltage becomes more negative, resulting in a monotonic decrease.

It has been shown that the worst-case recovery response of an n-channel transistor occurs for a zero volt bias during irradiation and a positive gate bias during the subsequent anneal [16]. This is true not only for the threshold voltage, by encouraging super recovery, but for mobility degradation as well, by maximizing the creation of interface state charges [16]; it is generally accepted that mobility is inversely proportional to the number of interface states [15,18,19]. A commonly used empirical relationship between mobility, μ, and the number of interface states, N_{it}, was proposed in 1984:

$$\mu = \frac{\mu_o}{1+\alpha \cdot \Delta N_{it}}, \qquad (2.1)$$

where α is a process dependent value and ΔN_{it} is dependent on dose and annealing conditions such as temperature and bias [18].

If an operating circuit were exposed to ionizing radiation, its devices would certainly be subjected to these biasing effects. The implication of such a situation is that the variation of performance or modeling characteristics may be non-uniform across the circuit. This greatly complicates the simulation of radiation-damaged circuits. What is generally done is to simply endow all of the simulated devices with the worst-case model parameters, regardless of the actual biasing conditions in the circuit. Although it is not exact, it is the most conservative approach.

Attempts have been made to streamline the simulation process. One of these is a program which was developed to analyze a circuit and determine its most sensitive subcircuits [20]. Worst-case bias conditions for each device in those weak links are then determined, the appropriate model parameter group as a function of dose is selected from a database, and each subcircuit is individually simulated for incremental doses. After finding the total dose at which failure occurs in each subcircuit, the smallest is taken to be the critical dose for the entire circuit. There are great computational savings in using this method, but by isolating circuit parts, the compounding of damage effects such as propagation delays is not allowed for. It is therefore possible that circuit failure would occur before the point that this approach predicts, a highly undesirable situation for inaccessible systems such as satellites. At any rate, this approach can assist the designer in determining critical paths and weak points in a design.

Another paper describes an algorithm which optimizes for delay and size of CMOS combinational logic circuits while accounting for total dose effects [21]. The optimization takes place at the transistor level, adjusting the individual geometries for an improved design. Once again, computational effort is at heart and switch-level simulation for the transistors is employed. The authors claim a one hundred-fold decrease in simulation time while sacrificing only ten

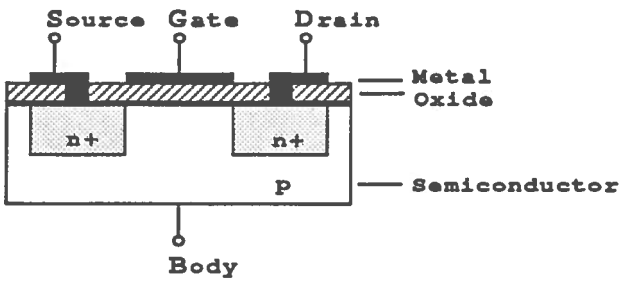
percent of the accuracy of a detailed SPICE simulation. Still, as is the case for all radiation-damaged circuit modeling approaches, an accurate library of key SPICE model parameters is relied upon.

CHAPTER 3

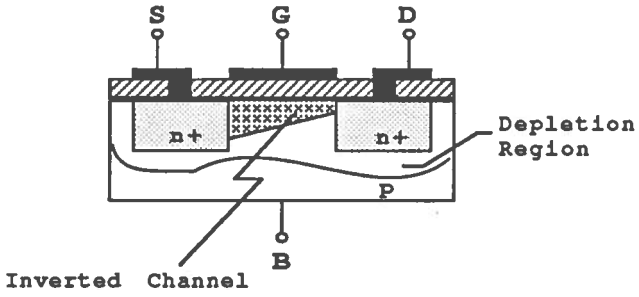
THEORY

The structure for a simple n-channel enhancement type MOSFET is shown in Figure 3.1(a). For this device, a conducting channel between the source and drain cannot be formed unless a sufficiently positive voltage is applied to the gate, with respect to the substrate and source. More specifically, as the gate-to-substrate and gate-to-source voltages are increased, holes are gradually driven away from the gate region and electrons are attracted to it. These electrons continue to accumulate just under the gate oxide between the source and drain. Eventually the number of electrons in the gate region greatly exceeds the number of holes, forming an n-type channel, and conduction can begin between the source and drain; the gate voltage at which this occurs is called the threshold voltage, V_T.

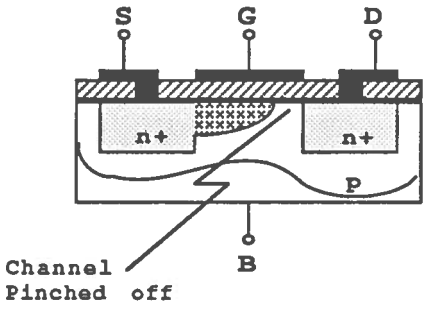
If the gate-to-source voltage (V_{GS}) is less than V_T, no channel is formed and the transistor is cut off. There exist two modes of operation if $V_{GS} \geq V_T$, depending on the drain-to-source (V_{DS}) biasing condition; these are illustrated in Figures 3.1(b) and 3.1(c). The horizontal component of the electric field is attributed to V_{DS}. For normal operation, this voltage is positive and electrons are swept from the channel to the drain. Furthermore, as V_{DS} increases, the shape of the channel changes. The increased resistive drop



(a)



(b)



(c)

Figure 3.1. The NMOS transistor
(a) Enhancement-type NMOS Structure
(b) Linear region: $V_{GS} > V_T$ and $V_{DS} \leq (V_{GS}-V_T)$
(c) Saturation region: $V_{GS} > V_T$ and $V_{DS} \geq (V_{GS}-V_T)$

across the channel can be observed in the current-voltage (IV) characteristic of Figure 3.2. While $(V_{GS}-V_T)$, the effective channel voltage, is greater than V_{DS} the device is said to be operating in the linear mode, as shown in Figure 3.1(b). In this mode, the drain-to-source current is a strong function of both V_{GS} and V_{DS}. If V_{DS} reaches a value such that $V_{DS} < (V_{GS}-V_T)$, the gate-to-drain voltage (V_{GD}) becomes less than V_T and the channel is said to be pinched off; see Figure 3.1(c). The length of the pinched-off region increases with V_{DS}, but the voltage drop across it remains constant at $(V_{GS}-V_T)$. When pinch-off occurs, I_{DS} becomes limited by the maximum velocity of the carriers in the strong electric fields. This effect can be seen in Figure 3.2.

There are a simple set of equations for ideal MOSFETs, the development of which will not be treated here.

$$V_{GS}-V_T \leq 0 : cut\text{-}off \rightarrow$$

$$I_{DS}=0 \tag{3.1}$$

$$0 < V_{DS} < (V_{GS}-V_T) : linear \rightarrow$$

$$I_{DS}=\beta \left[(V_{GS}-V_T) V_{DS} - \frac{V^2_{DS}}{2} \right] \tag{3.2}$$

$$0 < (V_{GS}-V_T) < V_{DS} : saturation \rightarrow$$

$$I_{DS}=\frac{\beta}{2} (V_{GS}-V_T)^2 \tag{3.3}$$

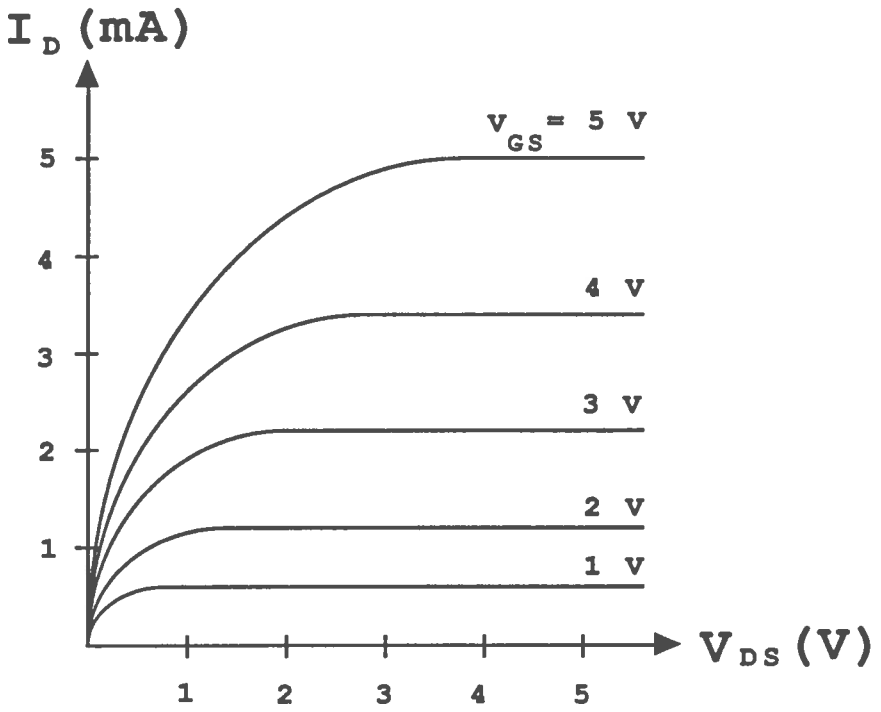


Figure 3.2. Typical NMOS I-V characteristic

In these equations, β is the device transconductance parameter. It is dependent on the transistor geometry (Figure 3.3) as well as the device processing conditions. Mathematically, β can be expressed as

$$\beta = \left(\frac{W}{L}\right) \cdot \frac{\mu\varepsilon}{t_{ox}}, \qquad (3.4)$$

where W is the width of the channel, L is the length of the channel, μ is the surface mobility of electrons in the channel, and t_{ox} is the thickness of the insulating oxide. The latter half of equation (3.4), $(\mu\varepsilon/t_{ox})$, is frequently grouped together as a single parameter: K_p, called the process transconductance parameter.

The current equation for the saturation region (3.3) assumes that I_{DS} saturates. In actuality, the drain current increases slightly as V_{DS} increases. An improved equation for the saturation region is:

$$I_{DS} = \frac{\beta}{2} \left[(V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \right] \qquad (3.5)$$

where λ is an empirical value for the channel length modulation factor.

Another phenomenon not yet mentioned is the body effect. This is a positive shift in the threshold voltage due to an increase in the source-to-substrate bias. It should be noted that a change in V_{SB} does not necessarily imply a change in V_{GB}. The total amount of positive charge above the gate does not change and therefore the total amount of negative charge

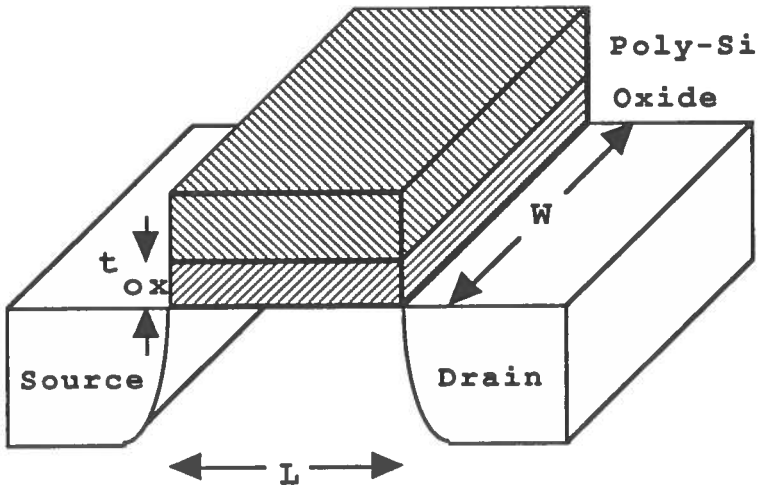


Figure 3.3. MOSFET geometry: oxide thickness, channel width, and channel length

under the gate remains the same. With that, consider that the source terminal is coupled directly to the n-channel, and below that channel is p-type material. This situation can be likened to a p-n junction whose degree of reverse bias is directly proportional to V_{SB}. As the depletion region of the reverse biased field-induced diode is widened, more of the p-type atoms are uncovered. The resulting increase in negative charge must be countered to maintain charge neutrality, i.e. to exactly balance the charge above the oxide. Thus, the level of inversion will decrease. This is the body effect, γ, and may be expressed as

$$\gamma = \left(\frac{t_{ox}}{\varepsilon_{ox}}\right)\sqrt{2q\varepsilon_{Si}N}, \tag{3.6}$$

where ε_{ox} is the permittivity of silicon dioxide, q is the charge on an electron, ε_{Si} is the permittivity of the silicon substrate, and N is the doping density of the substrate [22].

The body effect factor readily lends itself to an improved expression for threshold voltage:

$$V_T = V_{T0} + \gamma\left[\sqrt{V_{SB}+2\phi_F} - \sqrt{2\phi_F}\right], \tag{3.7}$$

in which ϕ_F is the Fermi potential of the substrate (a constant), and V_{T0} is the threshold voltage with V_{SB} equal to zero [22]. The zero bias threshold voltage is also a function of the body effect, as well as a couple of other notable parameters. It is in equation (3.8) that the effect of radiation damage on threshold voltage may be seen; ϕ_{MS} is

the metal-to-semiconductor work function and N'_{ss} represents the effective number of surface states per unit area in the device in question. For an NMOS transistor,

$$V_{T0}=\phi_{MS}-\frac{qN'_{ss}}{C'_{ox}}+2\phi_F+\gamma\sqrt{2\phi_F} \tag{3.8}$$

or, making the appropriate sign changes,

$$V_{T0}=\phi_{MS}-\frac{qN'_{ss}}{C'_{ox}}-2\phi_F-\gamma\sqrt{2\phi_F} \tag{3.9}$$

for a PMOS transistor [22]. Here, the assumption is made that all parasitic charges, such as oxide trapped and interface trapped charges, are located exactly at the oxide-semiconductor interface. If a device has charge trapped within the oxide, the value of this charge can be adjusted to an amount that would have the same effect at the interface. The composite charge is usually nets a positive value for both n- and p- channel devices, shifting the threshold voltage negatively.

Other variables in equation (3.8) include the oxide capacitance per unit area, C'_{ox}. C'_{ox} is a function of transistor geometry as well as oxide quality and may be expressed as

$$C'_{ox}=\frac{\varepsilon_{ox}}{t_{ox}} \tag{3.10}$$

where

$$\varepsilon_{ox}=k_{ox}\varepsilon_{o}. \qquad (3.11)$$

The quantity k_{ox} is the dielectric constant of the insulator, approximately 3.9 for SiO_2; the permittivity of free space, ε_o, is $8.86\text{x}10^{-14}$ F/cm.

Having now discussed the basic quantities in the modeling of MOSFETs, the issue of implementation in SPICE arises. There exist many model parameters in SPICE, whose Level Two and Three models are more sophisticated than those presented, which may be manipulated to describe devices. A large number of these are geometrical capacitances, such as C'_{ox}. The values, for those that change with bias, are unaffected by photon radiation. Other structural parameters which are insensitive to radiation are those such as oxide thickness, substrate doping, source and drain ohmic resistances, lateral diffusion of the ions implanted into the source and drain regions, the surface inversion potential $2\phi_F$, and of course the type of gate material. The remaining model parameters, some of which are of interest in radiation environments, have been summarized in Table 3.1.

The right hand column of Table 3.1 is concerned with the hypothesized radiation sensitivity of the model parameters relative to each other for the simulation of circuits. Some of these assignments were easy to make. It is widely accepted that threshold voltage and mobility are the modeling parameters most impacted by radiation damage; V_T is

Table 3.1. SPICE model parameters considered for radiation sensitivity study.

Symbol	SPICE Keyword	MOST Parameter Description	Radiation Sensitivity
V_{T0}	VT0	Zero-bias threshold voltage	High
K_P	KP	Transconductance parameter	Moderate
γ	GAMMA	Body-effect parameter	None
λ	LAMBDA	Channel-length modulation	None
N_{SS}	NSS	Surface state density	Moderate
N_{FS}	NFS	Fast surface state density	Moderate
N_{EFF}	NEFF	Total channel charge coefficient	None
μ_o	U0	Surface mobility	Moderate
U_c	UCRIT	Critical electric field for mobility	High
U_e	UEXP	Exponential coef. for mobility	Moderate
U_t	UTRA	Transverse field coefficient	None
υ_{max}	VMAX	Maximum carrier drift velocity	Moderate to Low
α_F	AF	Flicker-noise exponent	Low to None
K_F	KF	Flicker-noise coefficient	High

particularly sensitive since both interface and oxide charge buildup influence its value. With mobility caught in the middle, there is interplay between some of the parameters: an increase in the surface state density N_{SS} (with fast surface states N_{FS} being dominant [17, p. 196]) is the mechanism by which mobility degrades. Similarly, mobility is the only radiation-sensitive parameter in K_p. These four parameters (μ_o, N_{SS}, N_{FS}, and K_p) are therefore considered to be moderately sensitive to radiation damage.

Another parameter whose sensitivity may be readily evaluated is the body effect coefficient γ. None of the variables in equation (3.6) that compose γ are influenced by radiation. It is also assumed that the channel length modulation factor, λ, is insensitive to radiation as it is a substrate-oriented effect and is not a function of oxide or interface quality.

Though rarely significant in digital circuits, the element of flicker, or 1/f, noise can have dire consequences in an analog circuit. Evidence suggests that flicker noise is due to the presence of near-interfacial interface traps which can be created by ionizing radiation [23]. The flicker noise spectrum can be represented as

$$S_v = K_F \cdot \frac{V_d^2}{(V_g - V_t)^2} \cdot f^{-\alpha_F} \qquad (3.12)$$

where K_F is the normalized noise power, f is the frequency,

and α_f is a positive exponent approximately equal to one [23]. One of these two parameters, K_f, was shown to be a strong function of dose; in fact, a dose of 500 krad can result in an order of magnitude increase while the slope of the spectra does not noticeably change [23].

The final set of parameters to consider involve the mobility in the linear region. It was assumed for convenience that mobility remains constant with applied voltage in the derivation of equation (3.3). In reality, there is a slight reduction in mobility with an increase in the gate voltage applied; an increase in gate voltage results in an increase in the vertical component of the electric field. The carriers then tend to rattle against the oxide with greater frequency, thus crossing the channel more slowly. In order to simulate this effect, the following relation [22] is used:

$$KP' = KP\left(\frac{\varepsilon_{si}}{\varepsilon_{ox}} \cdot \frac{U_c t_{ox}}{(V_{GS} - V_{TH} - U_t V_{DS})}\right)^{U_e}. \qquad (3.13)$$

The critical value of the gate-to-channel field is U_c and above this value the device transconductance parameter decreases. This value should follow the threshold voltage shift as it is absolute, making U_c very sensitive to radiation. The degree to which drain voltage contributes to the gate-to-channel field is represented by U_t. Chosen to be between zero and one half, this value is a manifestation of substrate characteristics and is therefore considered to be

unaffected by radiation. Finally, U_e is chosen to fit the observed rate of mobility decrease with the applied gate voltage. If the interface state density increases, it serves reason to state that by increasing the exposure of the charge carriers to these traps, the degree of degradation of mobility would increase. The degree of sensitivity of U_e is therefore assigned a moderate value.

Of the sensitive parameters in Table 3.1, zero bias threshold voltage, V_{TO}, and mobility, μ, were targeted for study in this thesis. The extraction of these parameters can be simplified by choosing a single region, or mode, for transistor operation; operation in saturation region can be ensured by setting V_{GS} and V_{DS} equal. The governing expression in this region appears in equation (3.3). If the square root of equation (3.3) is taken, a linear equation results:

$$\sqrt{I_{DS}} = (V_{GS} - V_{TO}) \sqrt{\frac{\beta}{2}} \,. \qquad (3.14)$$

By measuring I_{DS} at known $V_{GS} = V_{DS}$ values and plotting the square root of that current versus the applied bias, one may extract the parameters of interest: V_{TO} from the x-axis intercept and $\sqrt{\beta}$ from the slope, as implied by equation (3.14). From β and equation (3.4), the effective carrier mobility in the saturation region may be calculated. If the threshold voltage were to shift, N'_{ss} could be readily calculated from equation (3.8) as the other quantities on the

right hand side of the equation remain constant. Therefore,

$$N'_{SS}(final) = N'_{SS}(initial) - \frac{C'_{ox}}{q} \cdot \Delta V_{T0}. \qquad (3.15)$$

This discussion has illuminated the theory involved in device modeling. Application of the models in SPICE can serve to tie the theoretical and practical worlds together. In particular, key model parameters may be experimentally extracted from devices for use in simulation. It was shown in the preceding discussion how this may be accomplished for those parameters which are thought to be reasonably sensitive to radiation exposure: V_{T0} and μ.

CHAPTER 4

MATERIALS AND METHODS

4.1 Overview

The experimental work was performed on nine identical LSU-designed test chips. Among other structures, the test vehicles contained arrays of variant geometry NMOS and PMOS transistors. The study focused on the 100 μm by 100 μm NMOS and PMOS devices as well as the 200 μm by 200 μm PMOS devices. Eight of the test chips were irradiated with 1.49 keV X rays at a high dose rate and incremental total doses. During the irradiation and annealing periods, the devices were unbiased. Following exposure, the zero bias threshold voltage, V_{T0}, and gain factor, β, were extracted from I-V measurements in the saturation region and analyzed for each transistor.

4.2 Test Chips and Devices

The test chips were fabricated by Orbit Semiconductor, Inc. using the MOSIS n-well processing technology using monies from a National Science Foundation grant to LSU. The chips arrived in a ceramic-type forty pin dual-in-line-package. Full view of a chip was be attained by removing a small metal plate, taped to the top of the package. A report containing the lot-averaged results of measurements performed on company test structures on selected wafers in the same lot

accompanied the chips. Also in the report were the sets of Level Two SPICE NMOS and PMOS model parameters, which were obtained by conducting similar measurements; see Tables 4.2.1 and 4.2.2.

An important point to make is that the Orbit test structures (kerf) were not necessarily in the same region of the wafer as LSU's test chips. As there are unknown process variations across the wafer, such as the ion implantation profile, it may expected that some of the device modeling parameters for the LSU devices differ from those of Orbit. In fact, K_p may vary as much as twenty percent for a given process [24].

The discrete devices in the test chip include both small (width and length less than 10 μm) and large geometry devices of NMOS and PMOS types. The gates, sources, drains, and bodies are accessible by probing 100 μm by 100 μm pads on the surface of the chip. Initial measurements conducted on the functional smaller geometry devices showed that the drains of some were shorted together. It was therefore decided to limit the study to three of the four large geometry devices on each chip: the 100 μm by 100 μm NMOS and PMOS devices as well as the 200 μm by 200 μm PMOS devices. None of the 200 μm by 200 μm NMOS devices were functional and the reason is unknown. A ground strap was used as a precaution during all chip handling operations to protect the devices from static hazards.

Table 4.2.1. Lot-averaged SPICE NMOS model parameters

NMOS Parameters		
LD=0.24974U	TOX=394.00001E-10	NSUB=2.296064E16
VTO=0.956762	KP=5.504E-5	GAMMA=0.9961
PHI=0.6	UO=628.787	UEXP=0.22018
UCRIT=115298	DELTA=1.041739E-5	VMAX=83151.5
XJ=0.25U	LAMBDA=1.67204E-2	NFS=2.509221E12
NEFF=1	NSS=1E10	TPG=1
RSH=27.36	CGDO=3.283217E-10	CGSO=3.28322E-10
CGBO=4.96808E-10	CJ=4.1066E-4	MJ=0.467277
CJSW=3.9772E-10	MJSW=0.334688	PB=0.8

Table 4.2.2. Lot-averaged SPICE PMOS model parameters

PMOS Parameters		
LD=0.25000U	TOX=394.00001E-10	NSUB=5.917000E15
VTO=-0.804571	KP=2.296E-5	GAMMA=0.5057
PHI=0.6	UO=262.000	UEXP=0.22505
UCRIT=21136.5	DELTA=.721685	VMAX=41563.6
XJ=0.25U	LAMBDA=5.597E-2	NFS=8.0389E11
NEFF=1.001	NSS=1E10	TPG=-1
RSH=70.00	CGDO=3.286622E-10	CGSO=3.28322E-10
CGBO=4.75120E-10	CJ=12.0692-4	MJ=0.431872
CJSW=1.9981E-10	MJSW=0.177313	PB=0.7

The use of large geometry devices eliminates a compounding of model parameter shifts due to short channel and narrow width effects, which are dependent on dose [25]. One drawback of using these particular devices, however, is that the sources are contacted to the substrate (PMOS) or the well (NMOS), as the case may be. This disallows a direct measurement of the body effect by the I-V technique as V_{SB} in equation (3.7) is always zero. It would have been a useful parameter to obtain for the purpose of correlating more of the data of this thesis with that of the manufacturer. But, since γ is itself assumed to be unaffected by X rays, this data is not critical.

4.3 X-Ray Exposure

The X-ray exposures were performed in an Airco Temescal Electron Beam Evaporator with an aluminum target. The operating conditions were as follows:

Excitation voltage: 10 keV

Beam Current: 75 mA

Chamber pressure: $\sim 6.4 \times 10^{-6}$ Torr

The $K_{\alpha 1}$ line for aluminum is at 1.4867 keV and an excitation voltage of only 1.560 keV, V_K, is required to create ionization in the K-shell [2, p.114]. For excitation voltages up to $6V_K$, the number of K_α photon emissions increases approximately as $(V-V_K)^2$ [2, p.115]. The L_α line for aluminum is at approximately 700 eV. This does not pose a

significant problem in spectrum purity though; a spectral evaluation of the X rays showed a negligible presence of 700 eV photons [26]. The reason for this is two-fold. First, at such low energies, self-shielding (within the aluminum target) significantly favors absorption of the lower energy photons [27]. Second, the bremsstrahlung yield in aluminum is low since it is a fairly low Z material. As a rule of thumb, the average fraction, f_β, of an electron's energy that is shed in the form of bremsstrahlung radiation may be approximated as

$$f_\beta \approx \frac{k \cdot Z \cdot E_{max}}{3000} \qquad (4.3.1)$$

where k is about 0.7×10^{-3} MeV^{-1}, Z is the atomic number of the absorber, and E_{max} is the maximum beta energy in MeV [2, p. 111]. For aluminum and a ten keV electron beam, f_β is about 3×10^{-8}. Therefore, for a ten keV excitation voltage, the emitted X rays are predominantly at 1.49 keV.

In performing an exposure, the metal cover of the chip's package was removed and the open package was attached to a mounting plate. Dosimetry film was fixed next to the chip by taping its corners to the mounting plate. A 2.85 μm nitrocellulose pellicle was then placed over the chip and its mount to shield secondary electrons. This assembly was positioned approximately one foot above the aluminum target, a vacuum was pulled, and the beam was turned on.

After the exposure was made, the system was allowed to cool for at least twenty minutes before repressurizing and opening; this prevented rapid oxidation of the target.

4.4 Dosimetry

Dose calculations were based on the assumption of a monoenergetic 1.49 keV X-ray source. The intent of the calculation was to provide an estimate of the surface dose required to result in a given dose to the gate oxide. A cross-sectional representation of the geometry used in this calculation appears in Figure 4.4. The top layer, omitted for clarity in previous sketches, serves the purpose of insulating transistor structures both electrically and from the elements.

In calculating the surface dose, the formulae used were derivatives of

$$D_t = D_o e^{-[(\frac{\mu}{\rho})\cdot\rho\cdot t]}, \qquad (4.4.1)$$

where D_o is the incident dose, D_t is the dose at a depth, t, into the device, (μ/ρ) is the mass attenuation coefficient, ρ is the density of the shielding material. The values of $(\mu/\rho)_{SiO2}$ and $(\mu/\rho)_{Si}$ used in calculation were 1104 cm^2/g and 542.8 cm^2/g, respectively [28]. Typically, the density of SiO_2 is 2.2 g/cm^3, while that of Si is 2.32 g/cm^3. Using these values, if the desired dose to the gate oxide was 0.8668 mJ/cm^2, or 10^6 rad, the required dose at the surface

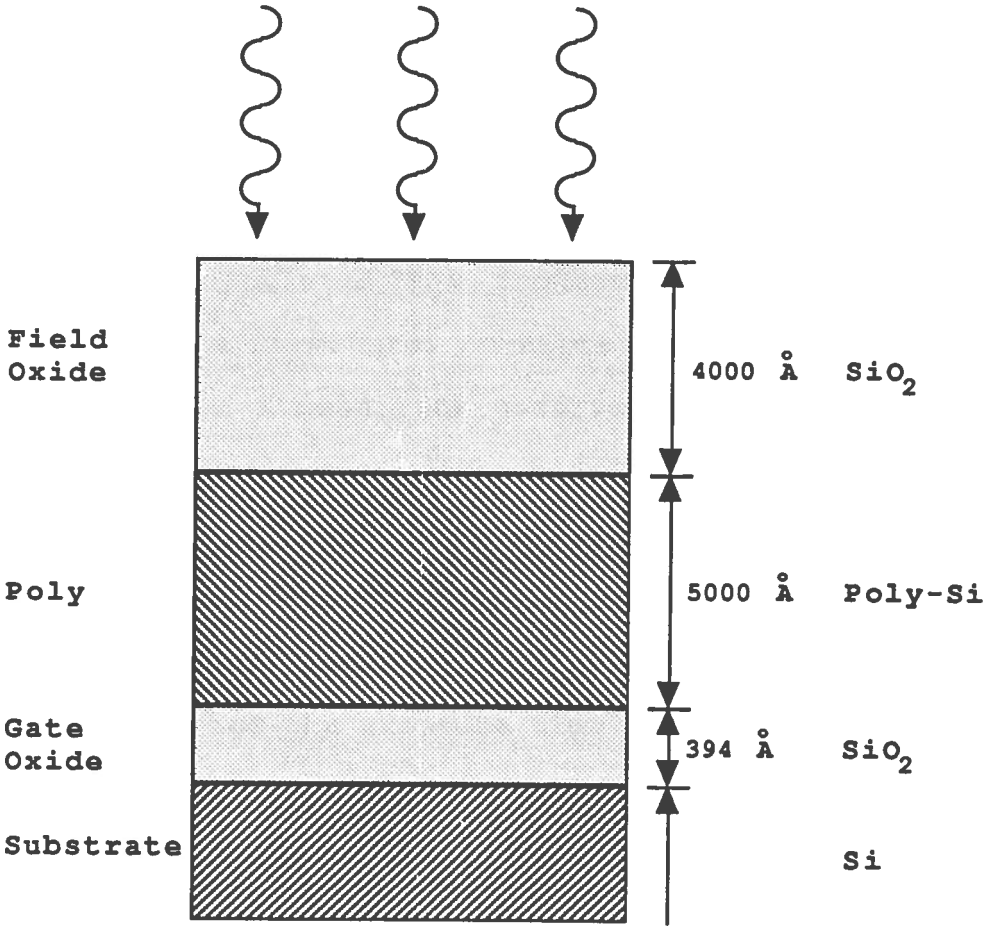


Figure 4.4. Shielding geometry employed

of the structure in Figure 4.1.1 is 10.68 mJ/cm^2. Notice that the exponential factor in equation (4.4.1) is independent of dose; this means that the incident dose may be linearly scaled for other gate oxide doses at the same depth in the same material. For example, if a two Mrad dose to the gate oxide were desired, the incident dose would be 2x10.68 mJ/cm^2 = 21.36 mJ/cm^2.

Having calculated the incident energy that must be absorbed in the structure, an approximate exposure time was calculated from a dose rate observed previously by another student. The initial exposure made use of this time and the dosimeter film was read in a Far West Optical Densitometer at a wavelength of 600 nm; it is presumed that the error in dosimetry was less than ten percent. Taking the ratio of the measured dose and the exposure time yielded the dose rate of the system; this was used to calculate subsequent exposure times. The results of the exposures may be viewed in Table 4.4.

As an added note, great care was taken to prevent exposure of the dosimeter film to ambient light in the laboratory both before and after X-ray exposure. Precautions included rapid transfer of the specimens between dark storage places and service areas. The transfers took place in the solid state laboratory under dim yellow light with the window blinds closed. Finally, the service areas were limited to the electron beam evaporator and the film reading facilities.

Table 4.4. Exposure and dose details for the eight irradiated test chips

Chip Number	Date of Exposure	Time of Exposure	Time in Field (min.)	Dose to Gate Oxide (Mrad)
0	11 Dec. 1992	11:00	7.00	0.76
3	11 Dec. 1992	13:30	14.00	1.55
1†	4 June 1992	n/a	n/a	2.0
7	14 Dec. 1992	11:00	24.00	2.63
8	14 Dec. 1992	13:30	34.00	3.66
2†	9 June 1992	n/a	n/a	4.0
4†	2 July 1992	n/a	n/a	8.9
5†	27 July 1992	n/a	n/a	17.1

(†) Exposures performed by Rajiv Nema under Dr. Ashok Srivastava

4.5 I-V Measurement and Parameter Extraction

In order to perform device measurements, it was necessary to place probes in contact with the microscopic terminal access pads. This was accomplished with a Signatone probing station, equipped with model SE-10T probes. The tip radius for these probes is 0.5 μm, necessitating extreme caution so as to avoid piercing the pads. Three probes were used: one for the gate pad, one for the drain pad, and one for the source/body pad.

Once contact was made to the Device Under Test (DUT) terminals, the devices could be exercised. A Hewlett-Packard 4140B pico- ammeter/DC voltage source was the instrument employed. The 4140B is controlled by an HP 362 microcomputer, facilitating the programmability of the 4140B and providing a hardcopy option for the data collected [29].

Early I-V measurements revealed the presence of two erroneous currents. The first of these was a photocurrent. A heavy black cloth was placed over the probing station and the room lighting was dimmed during subsequent device characterizations, eliminating the photocurrent altogether. The second source of error was noise. At a value less than 0.3 pA however, it was negligible.

Two sets of I-V data were collected for each of the devices studied both before and after irradiation, with an exception; the devices on board several chips in Table 4.4 entered this study after already having been irradiated. The

first data set was collected with V_{DS} equal to V_{GS}; provided that there was not a sign reversal in threshold voltage, this ensured that the devices remained in the saturation mode. Figure 4.5.1 is a block diagram of this experimental setup.

Drain current was measured and recorded for 0.2 volt V_{GS} increments, ranging from zero to five volts. In accordance with equation (3.14), a linear extrapolation down to the voltage axis yields the threshold voltage; since V_{SB} always equals zero, $V_T \equiv V_{T0}$. A sample plot is provided in Figure 4.5.2 and the corresponding I-V pairs in Table 4.5. In extracting the threshold voltage, use was made of both the plot and the raw data. Specifically, the extrapolation was performed by choosing two points in the data set from which to write the equation of a line. The x-intercept was then computed for the line. With algebra, the computation can be compressed into a single equation:

$$V_T = \frac{(V_L\sqrt{I_{Hm}} - V_H\sqrt{I_{Lm}})}{(\sqrt{I_{Hm}} - \sqrt{I_{Lm}})}, \qquad (4.5.1)$$

where $(V_H, \sqrt{I_{Hm}})$ and $(V_L, \sqrt{I_{Lm}})$ are the coordinates of the two chosen points, A and B, respectively; the subscript m indicates that the magnitude of the current should be used. As a final note regarding this equation, the magnitude of the current and voltage at point A should be greater than that of point B.

Consulting the data plot facilitates choosing the best points. As there were a number of data pairs available, a

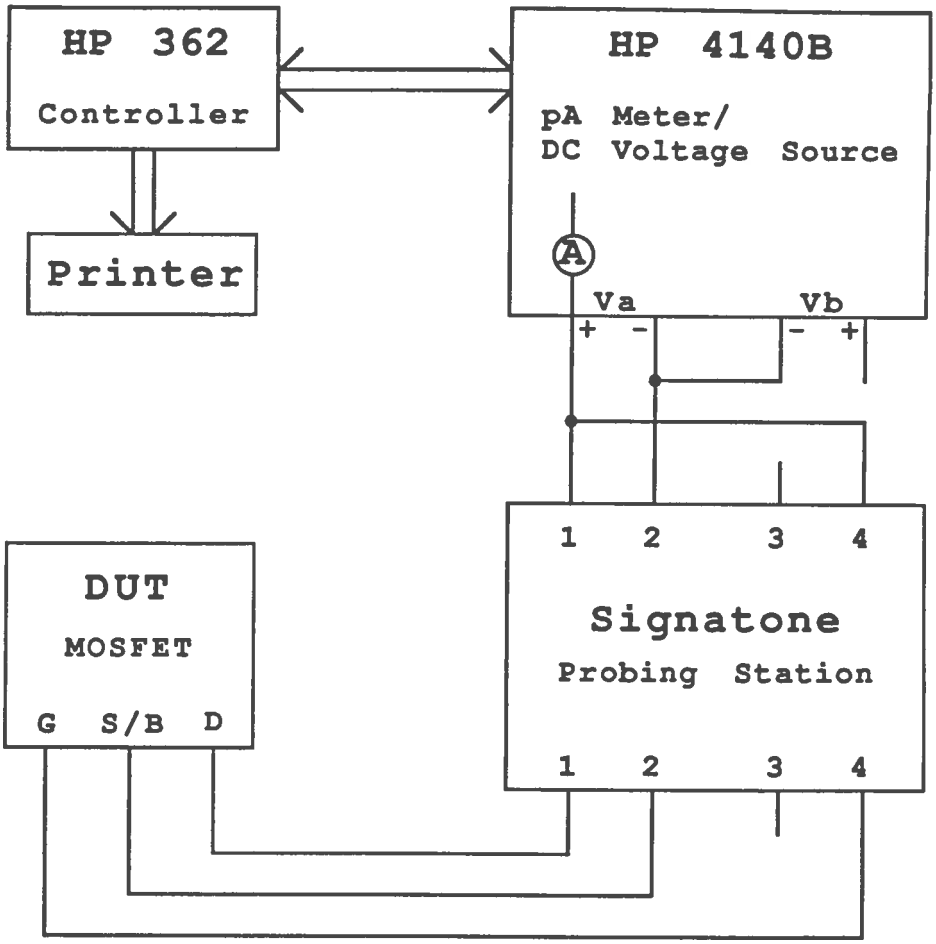


Figure 4.5.1. Block diagram of I-V measurement system for $V_{DS} = V_{GS}$

Table 4.5. Sample I-V data for an NMOS transistor in saturation.

$V_{GS} = V_{DS}$	I_{Dm}	$\sqrt{I_{Dm}}$
0.0	0	0
0.2	0	0
0.4	0	0
0.6	6.10E-10	2.47E-5
0.8	5.94E-8	2.44E-4
1.0	8.56E-7	9.25E-4
1.2	2.76E-6	1.66E-3
1.4	6.47E-6	2.54E-3
1.6	1.16E-5	3.40E-3
1.8	1.80E-5	4.24E-3
2.0	2.55E-5	5.05E-3
2.2	3.50E-5	5.92E-3
2.4	4.56E-5	6.75E-3
2.6	5.76E-5	7.59E-3
2.8	7.08E-5	8.41E-3
3.0	8.54E-5	9.24E-3
3.2	1.01E-4	1.02E-2
3.4	1.18E-4	1.09E-2
3.6	1.37E-4	1.17E-2
3.8	1.56E-4	1.25E-2
4.0	1.78E-4	1.33E-2
4.2	2.00E-4	1.41E-2
4.4	2.22E-4	1.49E-2
4.6	2.47E-4	1.57E-2
4.8	2.74E-4	1.65E-2
5.0	3.01E-4	1.73E-2

good deal of freedom was allowed in the selection. Examining the plot allowed a rough visual estimate of the threshold voltage. For consistency, the two points to be used in equation (4.5.1) were chosen to be one and three volts above the estimated threshold voltage. This was done because the slope V_{GS} versus the $\sqrt{I_D}$ curve is only approximately constant. The point selection process used helped minimize an error introduction as the threshold voltage shifted.

Another use for this first data set was the extraction of β. Beta can be computed after substituting the threshold voltage and a single I-V point in saturation into equation (3.3). Once again for consistency, the point chosen for this substitution was regularly three volts above the extracted threshold voltage. By such, any degradation in mobility, and thus beta, would be observed at the same bias, relative to the threshold. With the oxide thickness, channel length, channel width, and the device transconductance parameter known, equation (3.4) may be used to calculate the mobility.

The second data set extracted for each device was comprised of basic I_D-V_{DS} measurements for several values of V_{GS}, as in Figure 3.2. A block diagram of the setup used appears in Figure 4.5.3. These data would serve as a benchmark for simulation using the extracted device

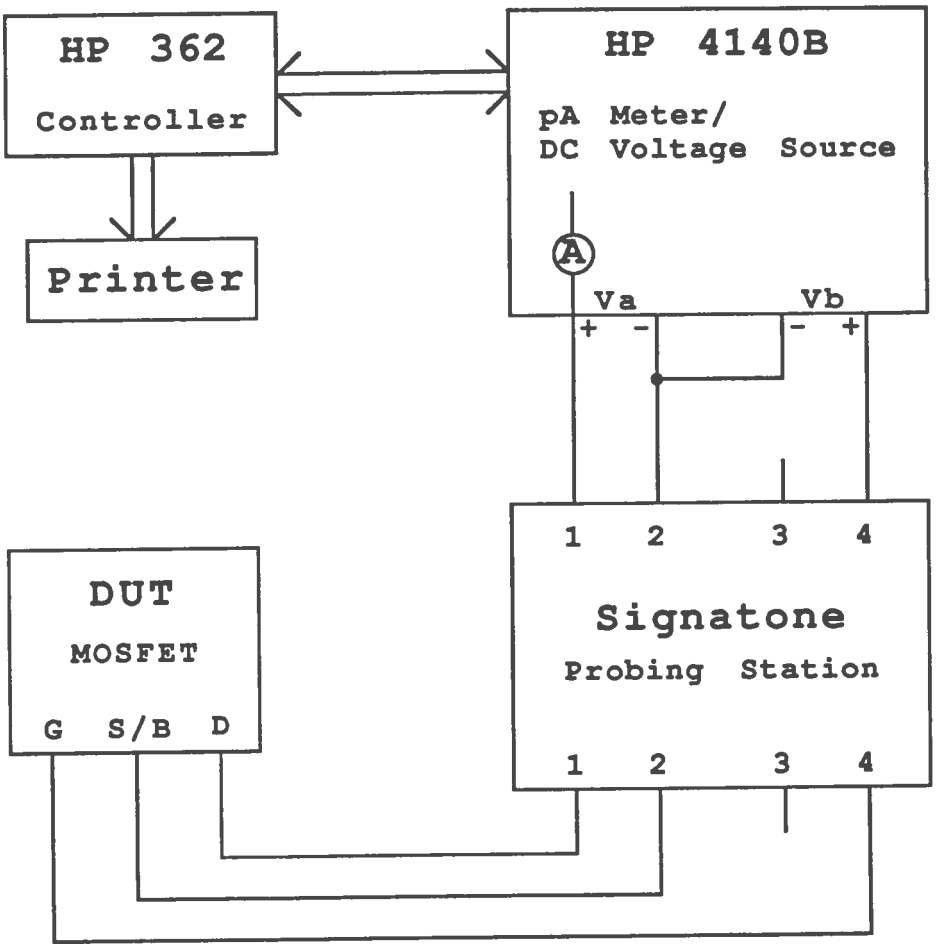


Figure 4.5.3. Block diagram of I-V measurement system for V_{DS} independent of V_{GS}

parameters. Another use for this particular data set was to make sure that the threshold voltage had not changed sign, forcing the transistor into a depletion mode and invalidating the assumption that the device was in saturation with $V_{GS}=V_{DS}$.

4.6 Annealing

The last consideration in the I-V measurement phase regards annealing. As reported in Chapter 2, the times, biases, and temperatures involved in the annealing period have been shown to be significant in a number of cases. The devices were unbiased and at room temperature during anneal; this minimized the annealing effects. Measurement dates and times are reported in Table 4.6 as are the absolute annealing times. Four of the integrated circuits were exposed prior to the initiation of this work and therefore had long annealing periods.

Table 4.6. Annealing details for the eight irradiated test chips

Chip Number	Date of I-V Measurement	Time of Measurement	Time Annealed (hours)	Dose to Gate Oxide (Mrad)
0	12 Dec. 1992	10:00	23.00	0.76
3	12 Dec. 1992	10:40	21.17	1.55
1†	14 Nov. 1992	10:00	3550	2.0
7	15 Dec. 1992	10:00	23.00	2.63
8	15 Dec. 1992	10:40	21.17	3.66
2†	14 Nov. 1992	10:40	3430	4.0
4†	14 Nov. 1992	11:15	2900	8.9
5†	14 Nov. 1992	11:45	2300	17.1

(†) Exposures performed by Rajiv Nema under Dr. Ashok Srivastava

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Overview

The results of the experimental work and its validation against simulation are presented in this chapter. The threshold voltage is shown to be in good qualitative agreement with theory, and the stability of the device transconductance parameter over the dose range employed indicates that the mobility is relatively insensitive to ionizing radiation. The extracted parameters are employed in SPICE simulations, validating their values by comparison to measured post-irradiation behavior. Finally, these results are applied in a hardened circuit design of a static ram cell.

5.2 Pre-irradiation Device Evaluation

The threshold voltage and device transconductance parameters for the devices unexposed at the onset of this work were extracted and appear in Tables 5.2.1 and 5.2.2, respectively. Deviation in threshold voltages is less than fifteen percent in all cases and differences in β for the PMOS devices are less than five percent. The device transconductance parameters for the NMOS transistors are not so uniform, however. A thirty-three percent difference exists at the extreme, owing its magnitude to the deviance of

Table 5.2.1 Pre-irradiation threshold voltages

Chip Number	V_{TO} (Volts)		
	NMOS 100 by 100 μm	PMOS 100 by 100 μm	PMOS 200 by 200 μm
6	0.726	-0.566	-0.541
0	0.762	-0.516	-0.507
3	0.789	-0.528	-0.544
1†	-	-	-
7	0.861	-0.467	-0.449
8	0.763	-0.530	-0.532
2†	-	-	-
4†	-	-	-
5†	-	-	-

(†) Data not available

Table 5.2.2 Pre-irradiation device transconductance parameters

Chip Number	β ($\mu A/V^2$)		
	NMOS 100 by 100 μm	PMOS 100 by 100 μm	PMOS 200 by 200 μm
6	33.622	12.516	12.442
0	34.117	12.435	12.295
3	36.212	12.464	12.690
1†	-	-	-
7	32.619	12.207	12.195
8	48.984	12.129	12.187
2†	-	-	-
4†	-	-	-
5†	-	-	-

(†) Data not available

the NMOS transistor of chip eight. This is an unusual condition, but it did not adversely impact the consistency of the results as will be shown in section 5.4.

5.3 Threshold Voltage

The extracted threshold voltages as functions of dose appear in Figure 5.3 and Table 5.3.1. The NMOS transistors exhibit the rebound (not super-recovery) condition discussed in the introduction. This condition is evidence of the creation of interface states. The PMOS devices also behaved much as a textbook would have them, excepting two points at the two Mrad level of exposure. As these devices were not characterized before irradiation, closely situated points are not in agreement, and PMOS devices are not known to exhibit a positive rebound from the buildup of interface states, these points have been considered anomalous. Finally, the shift in threshold voltages from the respective unexposed values is shown in Table 5.3.2 as a function of dose; these shifts are few in number and have therefore not been plotted.

5.4 The Device Transconductance Parameter and Mobility

Beta is shown as a function of dose for the NMOS and PMOS devices in Figure 5.4 and Table 5.4.1. The values for the PMOS transistors as a function of dose are almost constant, while those of the NMOS devices appear somewhat erratic between two and four Mrad. This may be explained by

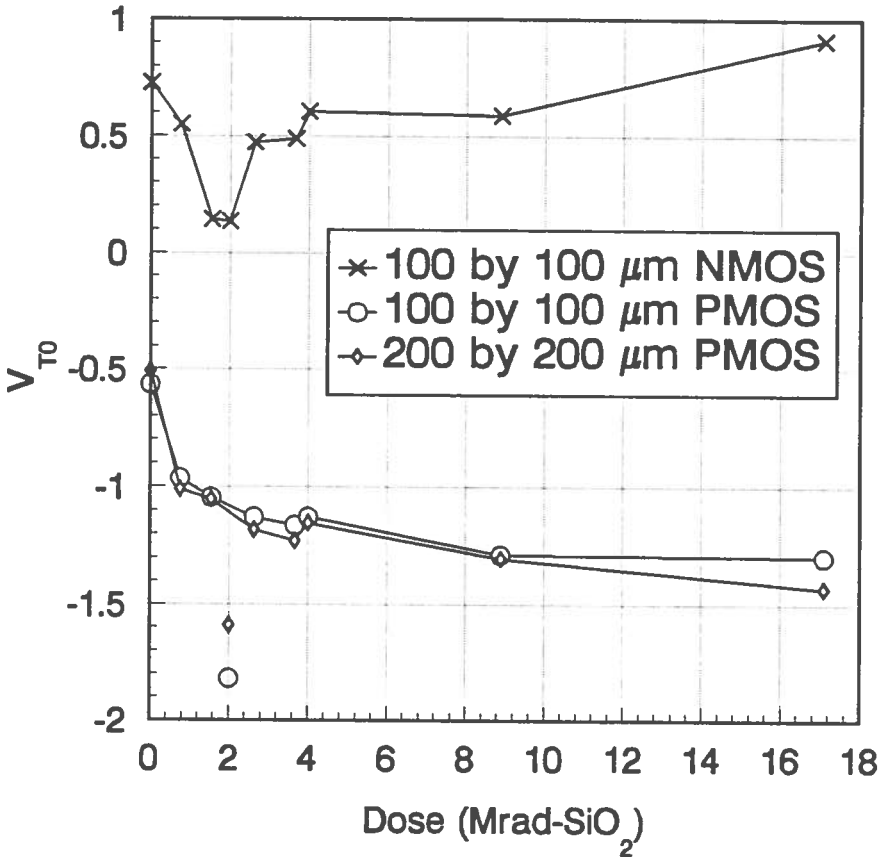


Figure 5.3. Zero bias threshold voltage shift vs. dose for 2μm MOSIS devices

Table 5.3.1 Threshold voltage versus dose

Chip Number	Dose (Mrad-SiO_2)	V_{T0} (Volts)		
		NMOS 100 by 100 μm	PMOS 100 by 100 μm	PMOS 200 by 200 μm
6	0.00	0.726	-0.566	-0.511
0	0.76	0.549	-0.965	-1.012
3	1.55	0.140	-1.046	-1.054
1	2.0	0.132	(-1.821)	(-1.591)
7	2.63	0.470	-1.130	-1.183
8	3.66	0.486	-1.163	-1.230
2	4.0	0.603	-1.129	-1.154
4	8.9	0.587	-1.288	-1.305
5	17.1	0.911	-1.298	-1.432

Table 5.3.2 Threshold voltage shift from pre-irradiated value versus dose

Chip Number	Dose (Mrad-SiO_2)	ΔV_{TO} (Volts)		
		NMOS 100 by 100 μm	PMOS 100 by 100 μm	PMOS 200 by 200 μm
6	0.00	0.00	0.00	0.00
0	0.76	-0.213	-0.449	-0.505
3	1.55	-0.649	-0.518	-0.510
1†	2.0	-	-	-
7	2.63	-0.391	-0.663	-0.734
8	3.66	-0.277	-0.633	-0.698
2†	4.0	-	-	-
4†	8.9	-	-	-
5†	17.1	-	-	-

(†) Data not available

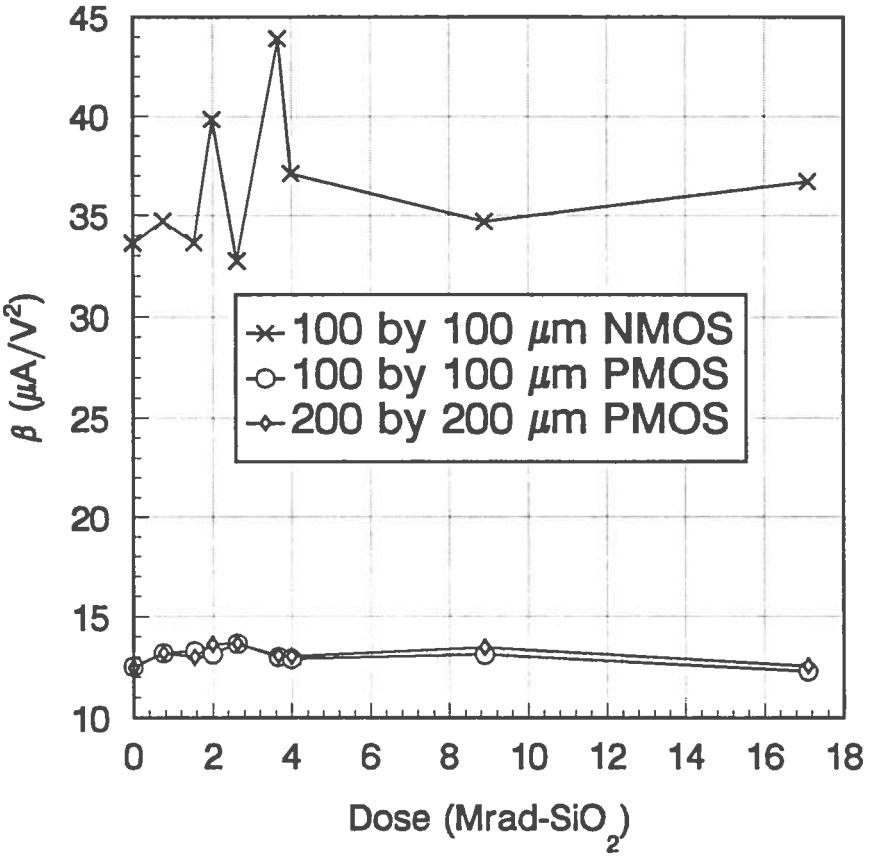


Figure 5.4. Gain factor vs. dose for 2μm MOSIS devices

Table 5.4.1 Device transconductance parameter versus dose

Chip Number	Dose (Mrad-SiO_2)	β ($\mu A/V^2$)		
		NMOS 100 by 100 μm	PMOS 100 by 100 μm	PMOS 200 by 200 μm
6	0.00	33.622	12.516	12.442
0	0.76	34.707	13.191	13.180
3	1.55	33.643	13.274	12.984
1	2.0	39.836	13.142	13.613
7	2.63	32.735	13.648	13.663
8	3.66	43.887	12.999	13.062
2	4.0	37.090	12.908	13.013
4	8.9	34.682	13.107	13.465
5	17.1	36.680	12.300	12.556

two observations: first, the high value at 3.66 Mrad is only five $\mu A/V^2$ lower than its large unexposed value; second, the pre-irradiated value of beta is unknown for the devices on chip one (two Mrad exposure). Discounting these anomalies, beta is stable over the given dose range for NMOS devices also. The actual measured shifts in the device transconductance parameters are listed in Table 5.4.2. Shifts are less than twelve percent and those which are positive are attributed to measurement error. Finally, since mobility is the only parameter defining β which is a function of radiation dose, and since β did not degrade significantly over the dose range used, mobility is insensitive as well. Because it is clear that interface states are being produced, the lack of a significant mobility degradation must be the result of the process-induced α value in equation (2.1) being small in magnitude.

5.5 Validation of Extracted Parameters

In order to demonstrate the effect of radiation upon the subjects of this experiment, Figures 5.5.1 and 5.5.2 have been included. These are I-V characteristic plots for a PMOS and a NMOS transistor before and after irradiation. It is apparent from the plots that the negative threshold voltage shift due to ionizing radiation serves to decrease the drain current in PMOS devices and increase the drain current in

Table 5.4.2 Device transconductance parameter shift from pre-irradiated value versus dose

Chip Number	Dose (Mrad-SiO_2)	$\Delta\beta$ ($\mu A/V^2$)		
		NMOS 100 by 100 μm	PMOS 100 by 100 μm	PMOS 200 by 200 μm
6	0.00	0.00	0.00	0.00
0	0.76	+0.590	+0.756	+0.885
3	1.55	-2.569	+0.810	+0.294
1†	2.0	-	-	-
7	2.63	+0.116	+1.441	+1.468
8	3.66	-5.097	+0.870	+0.875
2†	4.0	-	-	-
4†	8.9	-	-	-
5†	17.1	-	-	-

(†) Data not available

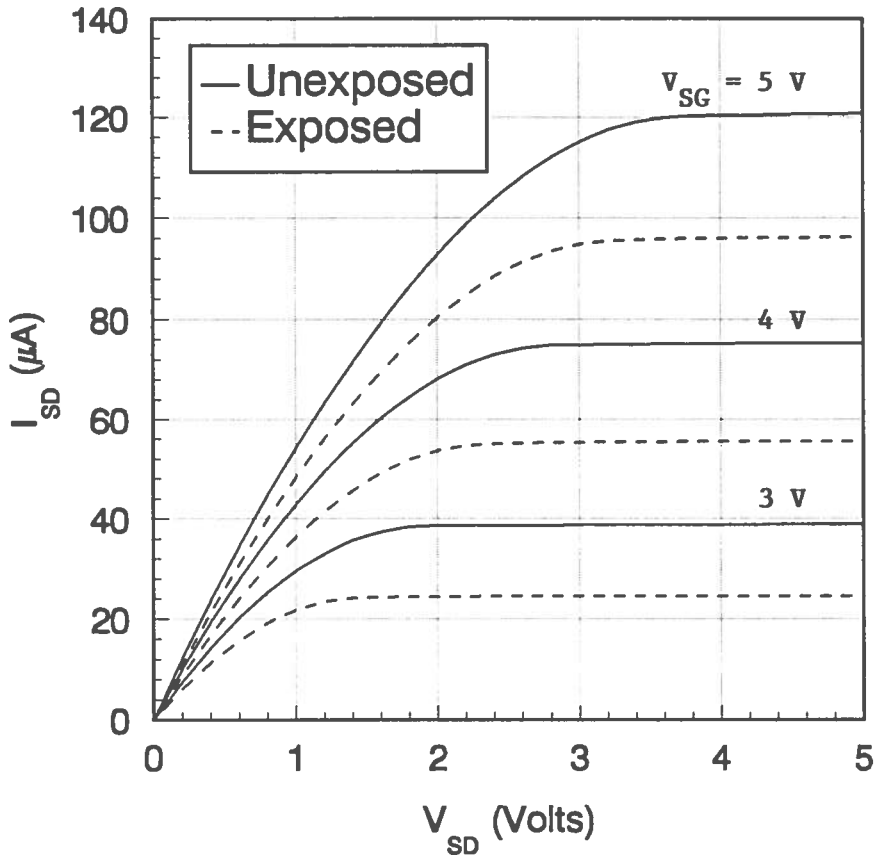


Figure 5.5.1. Measured I-V response of the 100μm by 100μm PMOS transistor of chip 7 before and after irradiation

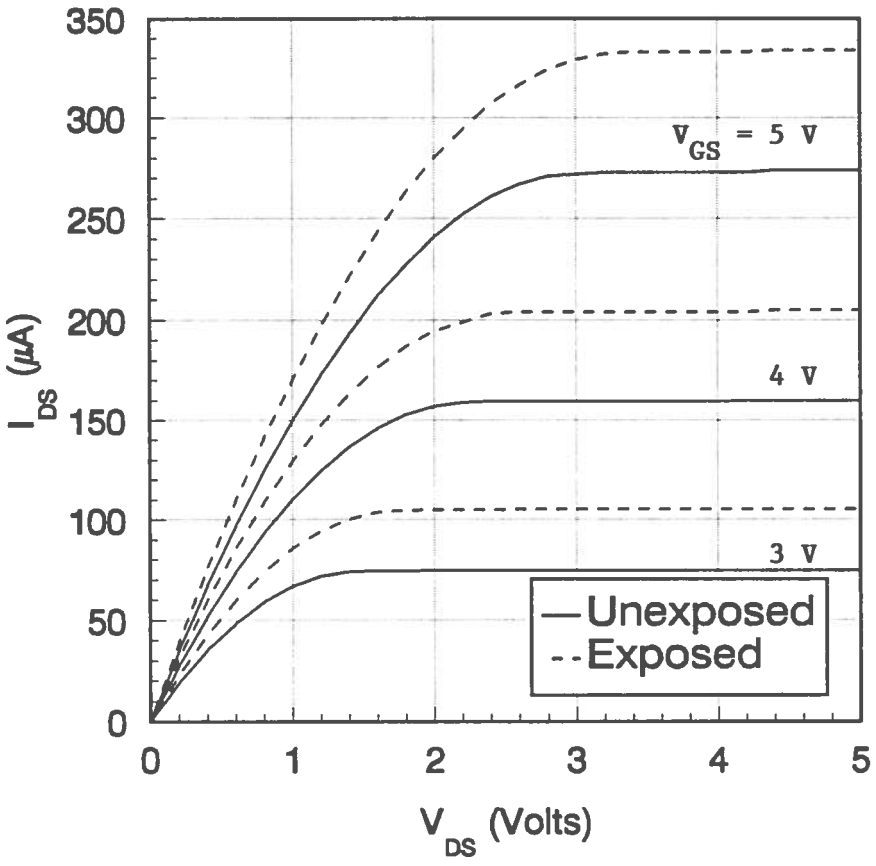


Figure 5.5.2. Measured I-V response of the 100μm by 100μm NMOS transistor of chip 8 before and after irradiation

NMOS devices. The magnitude of the PMOS transistor's threshold voltage increases with dose, making it more difficult to turn on, and the magnitude of the NMOS transistor's threshold voltage decreases with dose, making it easier to turn on; here, the ease of turning on refers to the magnitude of the gate-to-source voltage needed.

Simulations were conducted with SPICE for the same devices using the corresponding extracted pre-irradiated and post-irradiated threshold voltages and device transconductance parameters with the complementary parameters in Tables 4.2.1 and 4.2.2. The simulation output was superimposed on the empirically acquired data for each of the four cases: NMOS and PMOS, each unexposed and exposed to radiation. The results of these operations appear in Figures 5.5.3 through 5.5.6.

A significant discrepancy between measurement and simulation is evident for the PMOS devices (Figures 5.5.3 and 5.5.4). Examining these figures, the problem lies in the saturation region; such a large geometry device should not exhibit a significantly increasing current with applied source to drain voltage. As previously mentioned, the parameters used in simulation other than V_T and β included all of those supplied by the chip fabricator. Examining these, it is clearly a mistake to include the same λ (channel length modulation factor) as was extracted by the manufacturer for presumably small geometry devices. In fact,

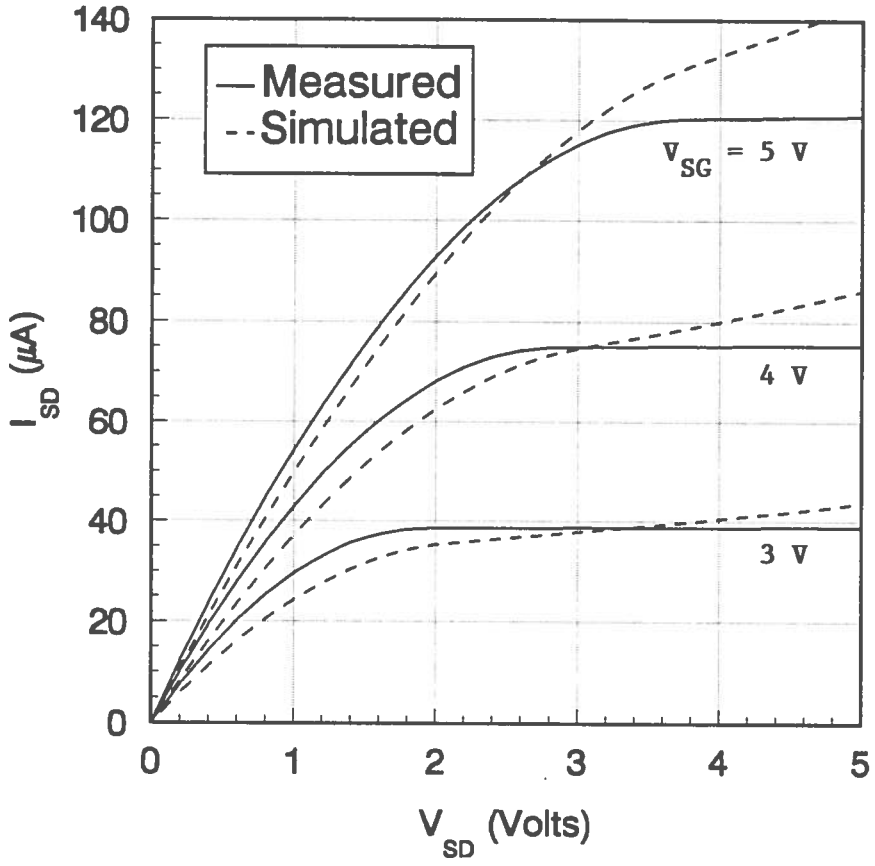


Figure 5.5.3. Measured and simulated I-V responses of the 100μm by 100μm PMOS transistor of chip 7 before irradiation

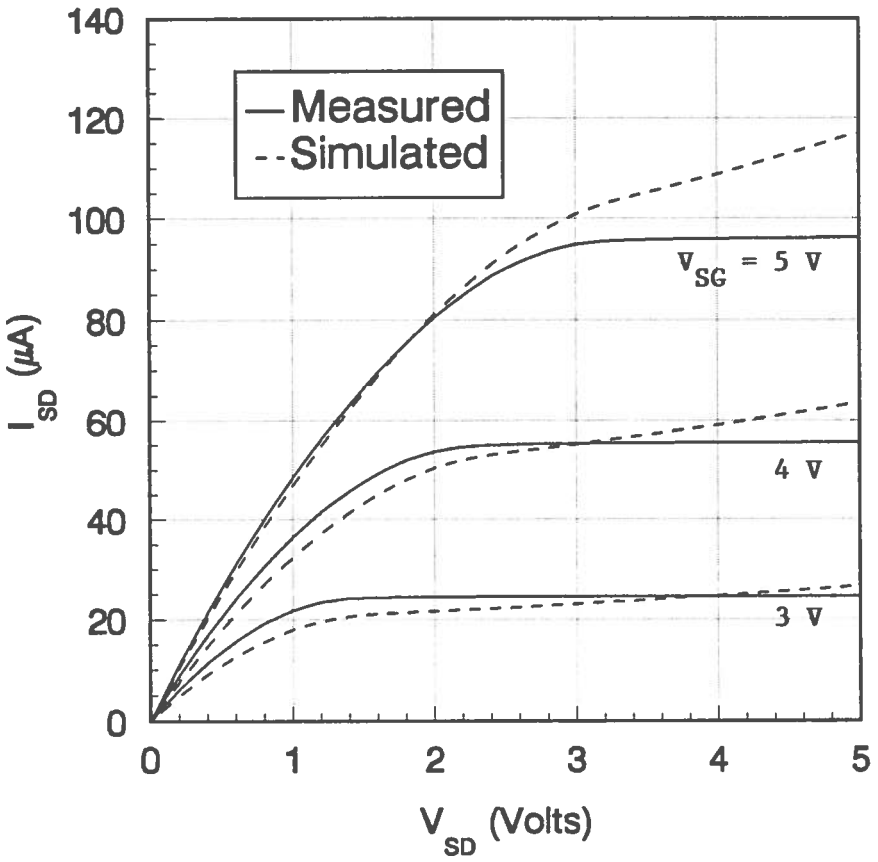


Figure 5.5.4. Measured and simulated I-V responses of the 100μm by 100μm PMOS transistor of chip 7 after irradiation

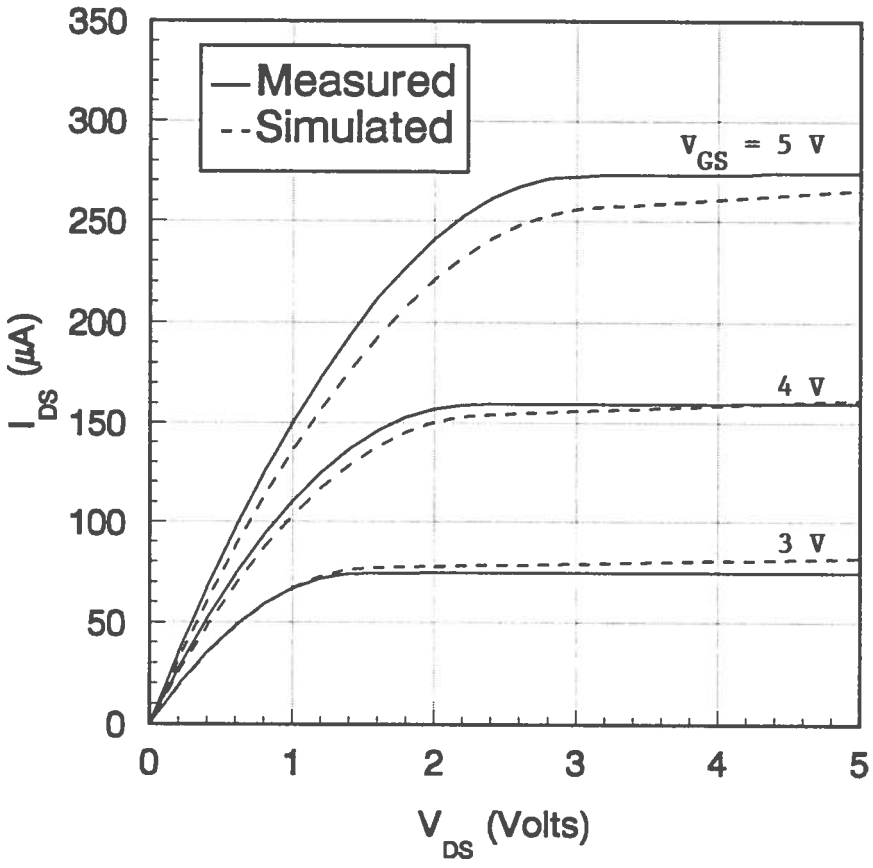


Figure 5.5.5. Measured and simulated I-V responses of the 100μm by 100μm NMOS transistor of chip 8 before irradiation

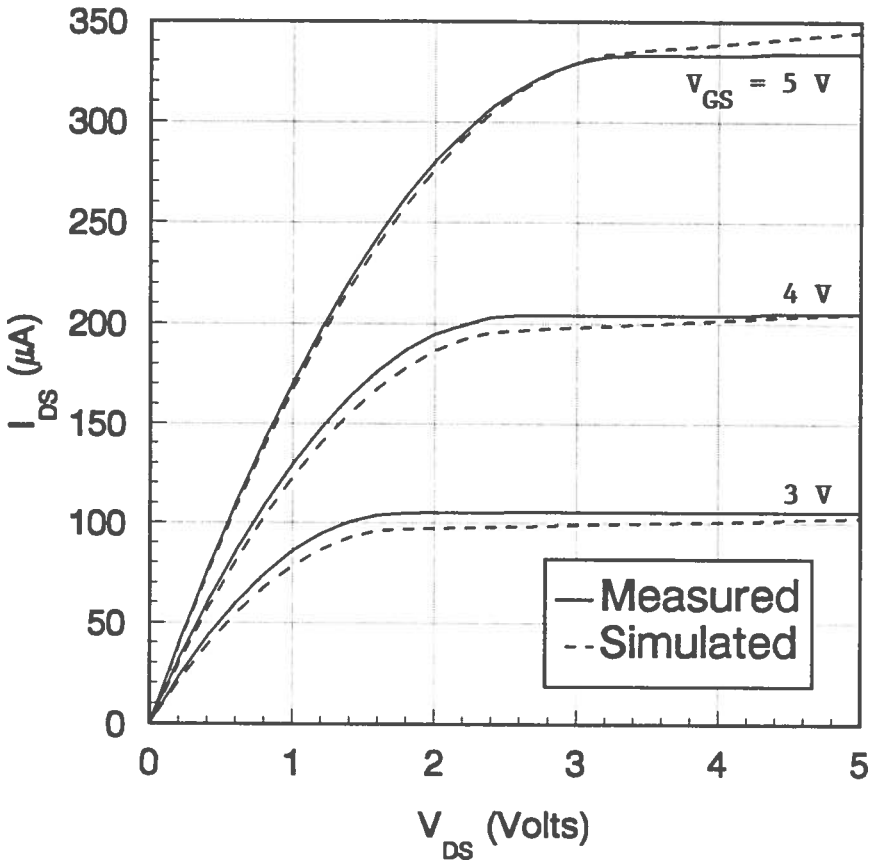


Figure 5.5.6. Measured and simulated I-V responses of the 100μm by 100μm NMOS transistor of chip 8 after irradiation

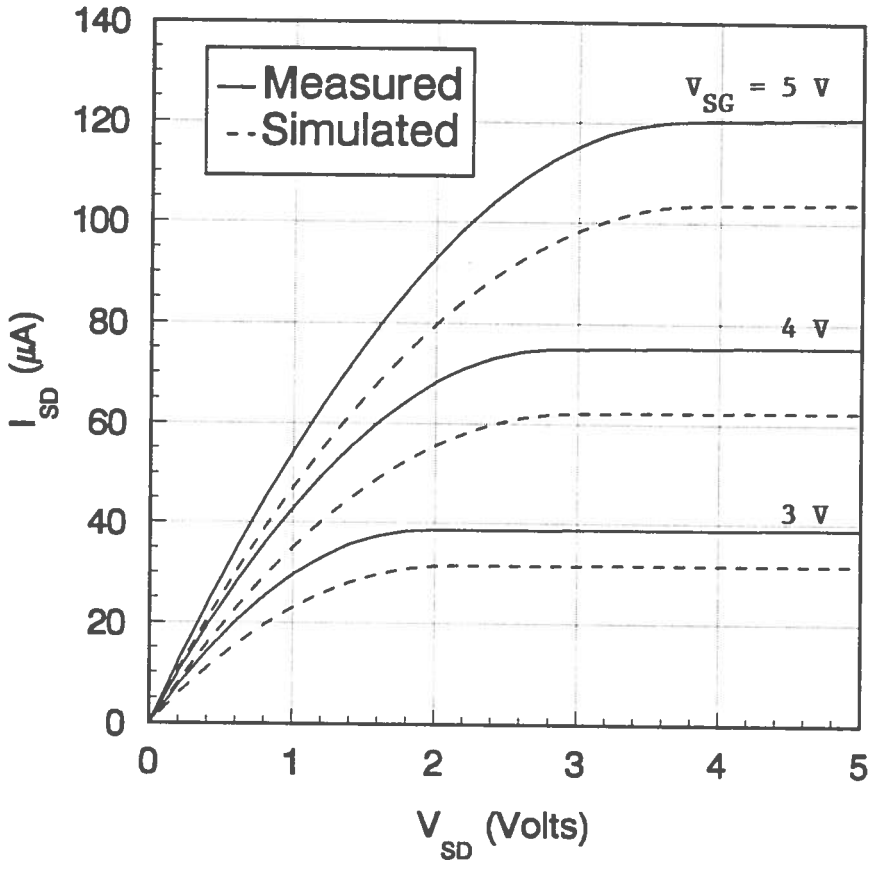


Figure 5.5.7. Measured and simulated I-V responses of the 100μm by 100μm PMOS transistor of chip 7 before irradiation and with lambda = 0

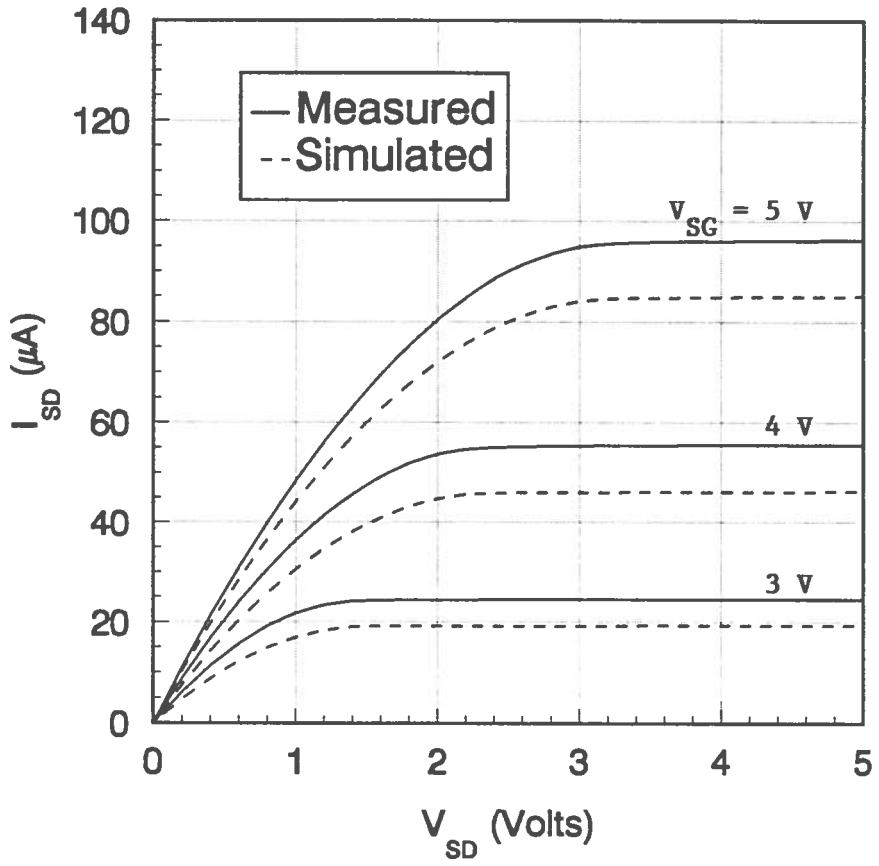


Figure 5.5.8. Measured and simulated I-V responses of the 100μm by 100μm PMOS transistor of chip 7 after irradiation and with lambda = 0

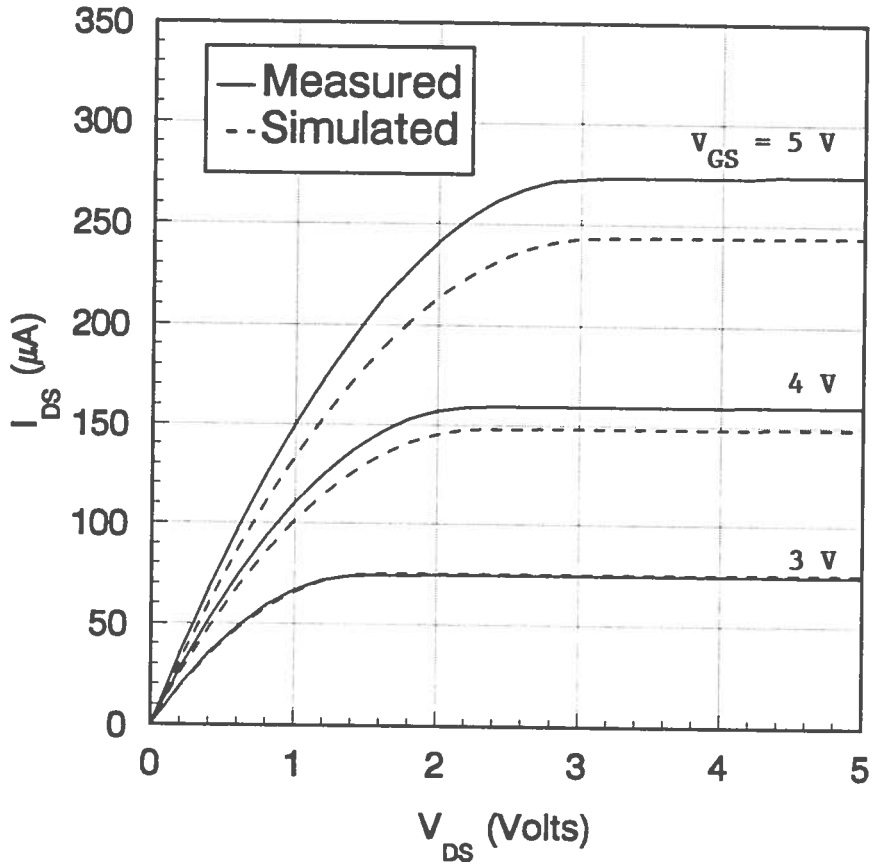


Figure 5.5.9. Measured and simulated I-V responses of the 100μm by 100μm NMOS transistor of chip 8 before irradiation and with lambda = 0

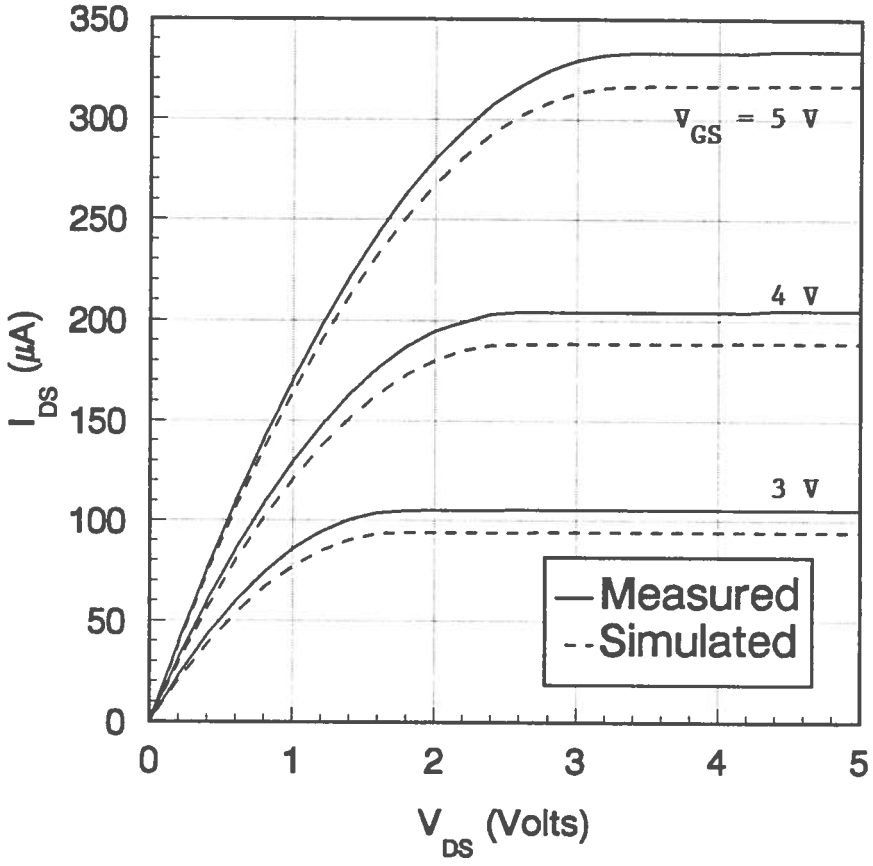


Figure 5.5.10. Measured and simulated I-V responses of the 100μm by 100μm NMOS transistor of chip 8 after irradiation and with lambda = 0

this factor is practically insignificant for long channel devices as may be seen in the measured data. To further validate the truth of this statement, the simulations were conducted again with lambda set equal to zero for both the NMOS and PMOS devices and the other parameters unmodified.

Figures 5.5.7 through 5.5.10 hold the results of this change. As it turns out, there is at most a ten to twenty percent underestimation of drain current in saturation. On a more positive note however, not only does the qualitative nature of the simulation mesh well with the empirical data, the underestimate is rather uniform across each device and situation.

The channel length modulation factor was therefore at fault as it is imperative that a model must first match its subject's qualitative behavior. The reason that the erroneous effect was more pronounced in the p-channel devices than the n-channel devices is that the effective doping level is less in the n-well than the in the substrate; lambda is less for the n-channel than the p-channel. This incorrect parameter makes an interesting point, however: it is possible that other model parameters may be incorrect in the simulation, resulting in the underestimated current. Device geometry is only one of the factors that could cause this type of deviation. For various reasons, some of the model parameters may deviate from those of the manufacturer's test devices. Additionally and most importantly, not all of the

radiation sensitive parameters in Table 3.1 have been extracted. In conjunction with measurement error, a fifteen to twenty percent compounded discrepancy between experimental and simulated device behavior is within reason.

5.6 CMOS Circuit Design for Hardness

The issue of radiation hardness is one of great concern when integrated circuits, such as SRAMs, are to be placed in hostile environments. This hardness is a function of device processing conditions and device sizing [21], as well as the layout and design of the circuit [30,31]. It was demonstrated that the MOSIS process exhibits radiation hardened properties. As a means of making use of this observation, a modified SRAM design is proposed herein and is based on the two micron MOSIS fabrication process.

Design for hardness presents no shortage of engineering tradeoffs. With regard to static memory devices, decoding logic design readily lends itself to the optimization methods of [21] and [30]. A more recent development shows that CMOS circuitry can be greatly desensitized to radiation [31]. The idea is the inclusion of compensation circuitry to counteract the problem of a decreasing zero input noise margin, which is the result of a decline in the threshold voltage of the n-channel device(s); a modified inverter is shown in Figure 5.6.1 [31].

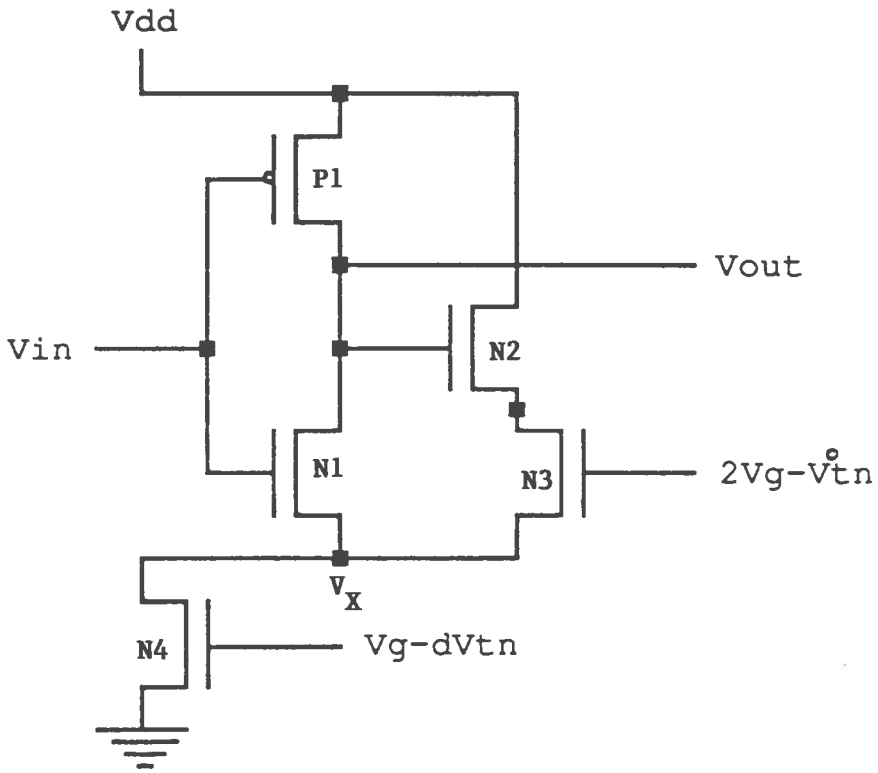


Figure 5.6.1. Modified inverter design [31]

The decreased noise margin is accompanied by a decrease in the state switching voltage, or inversion voltage. It may be shown that the inversion voltage of an inverter is:

$$V_{INV}=\frac{V_{DD}-|V_{Tp}|+V_{Tn}\sqrt{\beta_N/\beta_P}}{1+\sqrt{\beta_N/\beta_P}}. \qquad (5.6.1)$$

Similarly, analysis of an inverter with compensation circuitry shows:

$$V_{INV}=\frac{V_{DD}-|V'_{Tp}|+V_{Tno}\sqrt{\beta_N/\beta_P}}{1+\sqrt{\beta_N/\beta_P}}, \qquad (5.6.2)$$

where the prime indicates the post-irradiation value and V_{Tno} is the NMOS threshold voltage prior to irradiation; this derivation is an extension of the work in [31] and is included in Appendix A. A comparison of equations (5.6.1) and (5.6.2) reveals that the modified circuit's inversion voltage and noise margin are immune to shifts in V_{Tn}.

Though this can extend the useful life of a CMOS circuit in a radiation environment, there are drawbacks: there is generally a three transistor overhead for each independent gate or complex function and an additional seven transistor overhead for the chip as a whole, due to the need for two hardened constant/compensating current sources shared chip-wide. Additionally, the modification assumes no mobility degradation for either n- or p-channel devices. The authors of [31] did not address the beta ratios of transistors two and three in Figure 5.6.1; see Appendix B for its development.

The extra overhead translates into a significant area compromise, roughly a 100% increase for SRAMs, while the need for a stable mobility relies on processing conditions to eliminate mobility induced current drifts and timing faults. In extremely harsh environments, however, the area sacrifice may be tolerable. This modification also introduces an increase in static power dissipation; it is countered by a dramatic decrease in dynamic power dissipation, however. The voltage and current envelopes of unexposed simple and modified inverters in Figures 5.6.2 and 5.6.3 illustrate the savings.

If the devices had been biased positively during exposure, the V_T shift in the n-channel transistor could have been somewhat greater, driving it into a depletion mode. This situation was also simulated for both standard and modified inverter circuits. The simulated voltage and current transfer characteristics from this simulation appear in Figures 5.6.4 and 5.6.5. A comparison of these transfer characteristics with the previous set clearly demonstrates the superiority of the modified circuit in terms of both switching voltage and power dissipation.

A modified static memory cell, incorporating compensation circuitry, was designed for this thesis and appears in Figure 5.6.6. By inclusion of the compensation circuitry in both the memory and support circuitry, the terminal dose to an SRAM chip would be determined by the

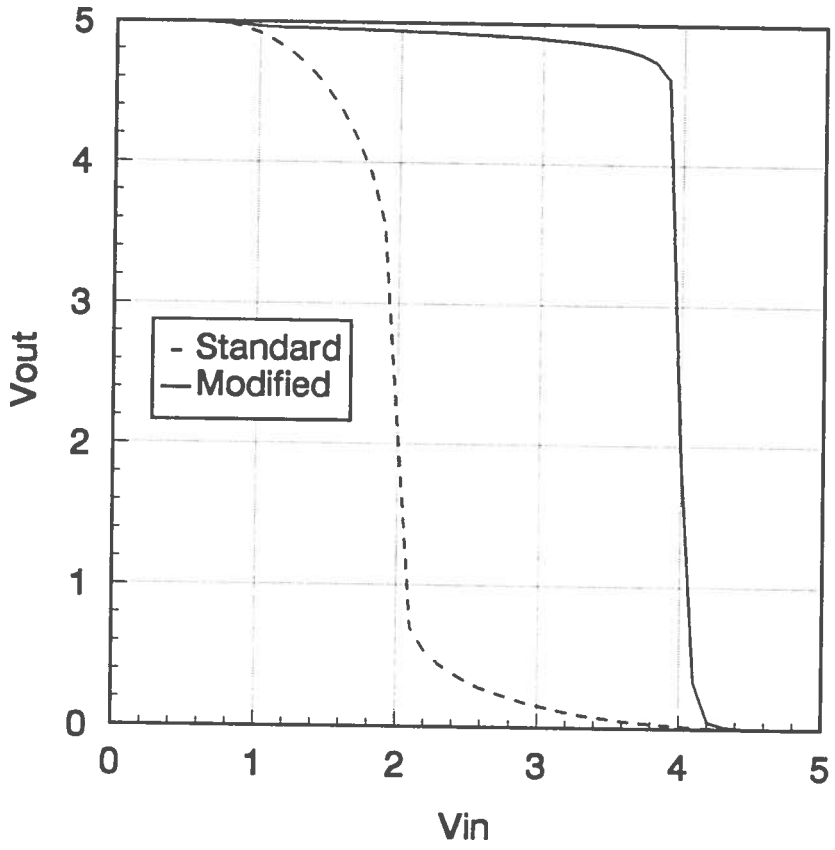


Figure 5.6.2. Simulated voltage-voltage transfer characteristics for unexposed inverters with Vtn=0.73V, Vtp=-0.57V : Standard design with Vinv=1.95V ; Modified design with Vg=0.8, dVtn=0.0V, and Vinv=3.97V

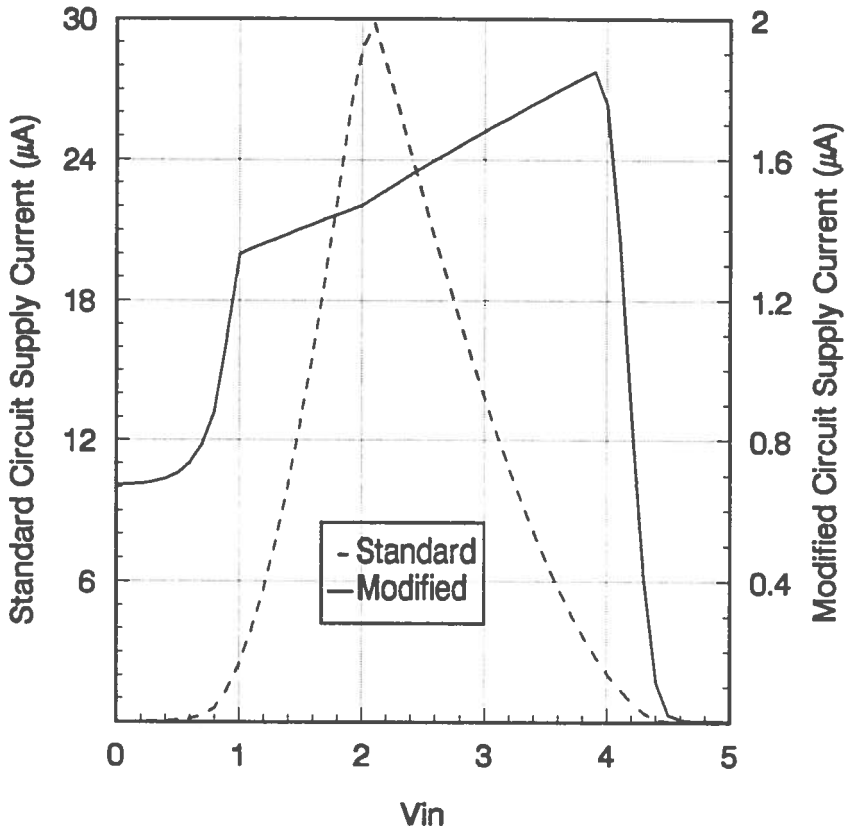


Figure 5.6.3. Simulated voltage-current transfer characteristics for unexposed inverters with Vtn=0.73V, Vtp=-0.57V : Standard design with Vinv=1.95V ; Modified design with Vg=0.8, dVtn=0.0V, and Vinv=3.97V

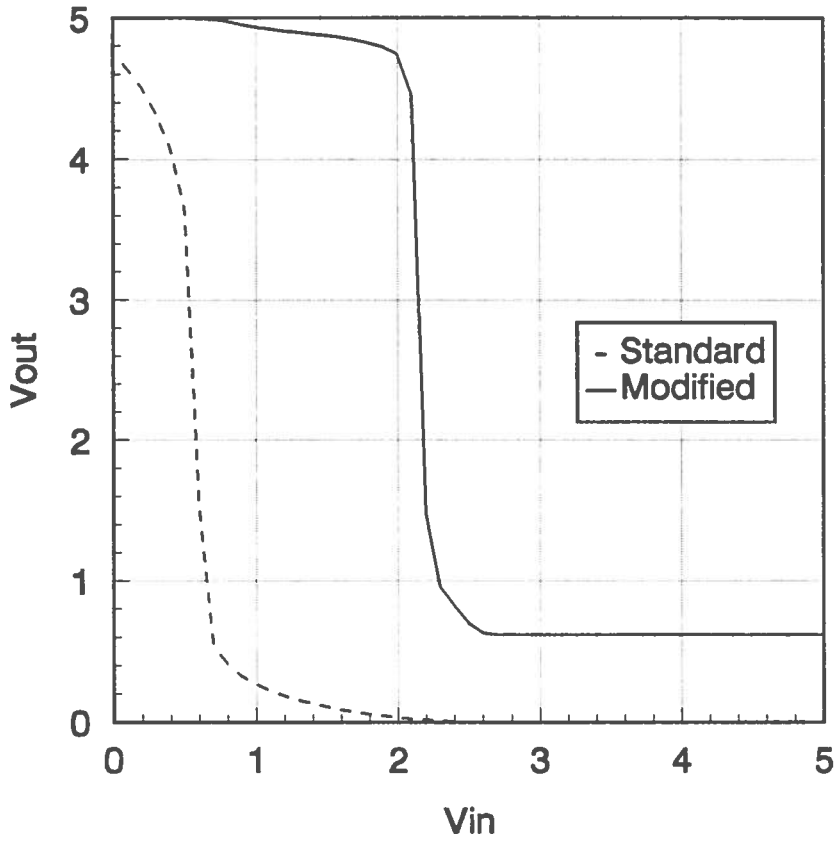


Figure 5.6.4. Simulated voltage-voltage transfer characteristics for radiation damaged inverters with Vtn=-0.50V, Vtp=-2.40V : Standard design with Vinv=0.53V ; Modified design with Vg=0.8, dVtn=1.23V, and Vinv=2.19V.

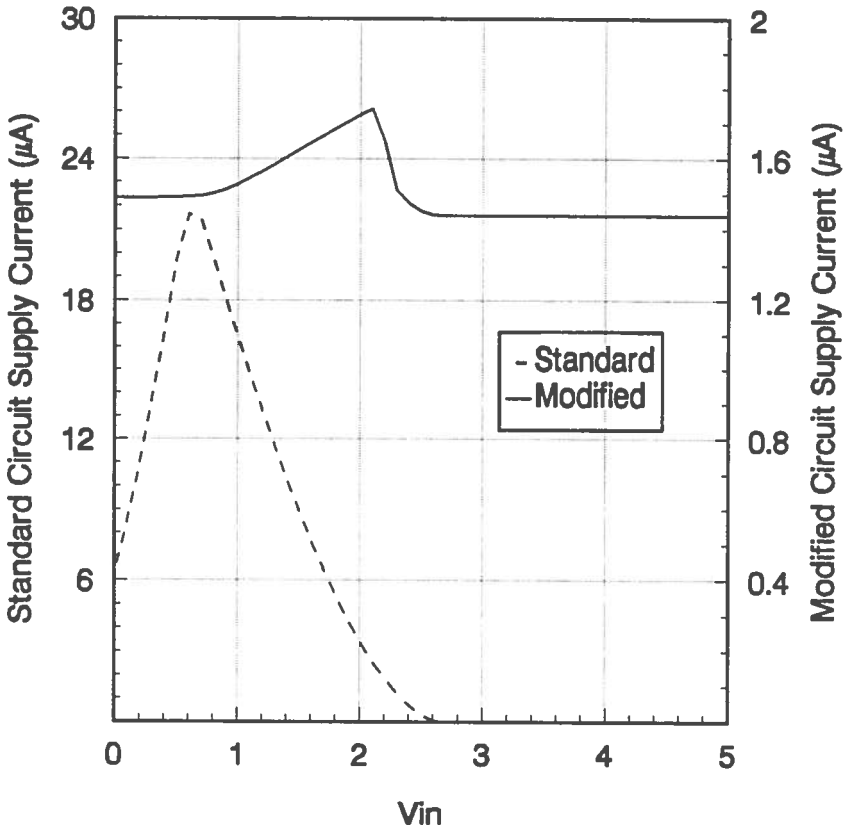


Figure 5.6.5. Simulated voltage-current transfer characteristics for radiation damaged inverters with Vtn=-0.50V, Vtp=-2.40V : Standard design with Vinv=0.53V ; Modified design with Vg=0.8, dVtn=1.23V, and Vinv=2.19V

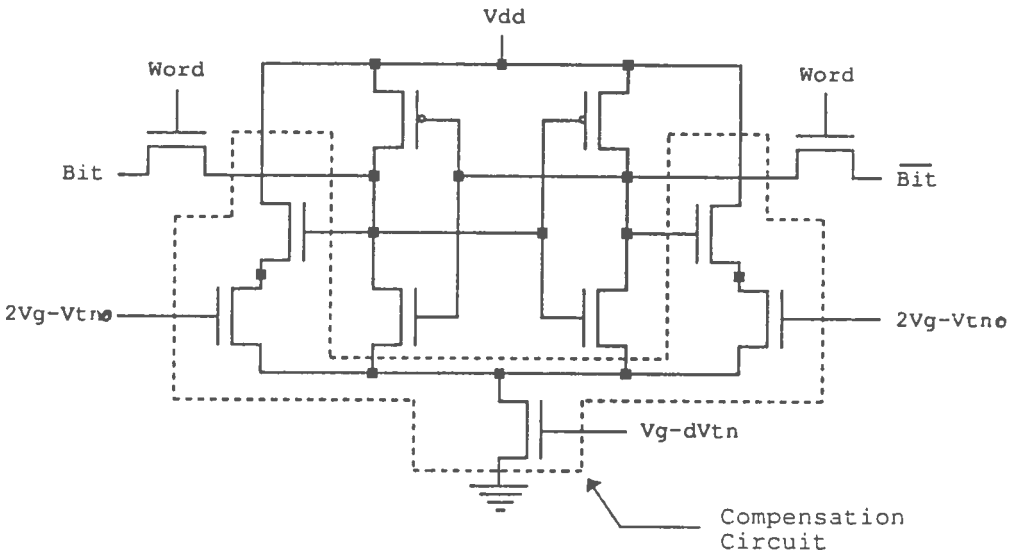


Figure 5.6.6. Radiation hardened SRAM cell

value at which the PMOS transistors become difficult to turn on; the output high, V_{OH}, must be maintained above 3.5 to 4 volts to assure the turning on of any n-channel devices. This dose is much greater than the traditional limiting dose at which excessive power dissipation, due to depletion mode NMOS transistors, results in catastrophic failure.

To conclude, the circuit design is such that the cell is insensitive to NMOS threshold voltage degradation. It is ensured that the transistor gain factor, ß, is influenced minimally by unbiased radiation exposure and that the n-channel devices remain in enhancement mode by utilizing MOSIS processing technology. When chip area can be compromised or weight is a concern, this design offers a viable alternative to increased shielding.

CHAPTER 6

SUMMARY AND CONCLUSIONS

6.1 Summary

Radiation damage to CMOS circuits can seriously alter their function. Threshold voltages and device transconductance parameters were extracted from NMOS and PMOS devices, fabricated using the MOSIS two micron process, which were exposed to 1.49 keV X rays. Dose commitments to the gate oxides ranged from 0.76 Mrad to 17 Mrad. The MOSIS two micron processing technology was shown to provide a degree of inherent hardness to radiation. The device transconductance parameter, and therefore the surface mobility, is stable over the dose range employed. Also, though the threshold voltages did shift, all of the devices remained in enhancement mode. These properties are desirable and were exploited in this thesis by designing a radiation hardened static memory cell. This memory cell includes circuitry which compensates for the radiation induced degradation of the n-channel transistor threshold voltage, thereby maintaining the lower noise margin.

6.2 Conclusions

- Annealing of trapped charges is negligible for unbiased devices over a five month period
- Postirradiation buildup of interface states is not encouraged for unbiased devices
- Interface states were created, as evidenced by the rebound of n-channel threshold voltages
- The process-dependent α value in mobility degradation is small for the MOSIS process
- Caution must be exercised regarding the use of the manufacturer's empirical geometry-dependent model parameters
- V_T and β extractions provide adequate simulation accuracy for digital circuits
- Additional SPICE model parameters should be extracted for the simulation of analog circuits: UCRIT, UEXP, VMAX, AF, and KF
- The MOSIS two micron technology is well suited for use in a new radiation hardened static memory design, insensitive to n-channel threshold voltage degradation

REFERENCES

[1] XCOM. A microcomputer program to compute cross-sections for interactions for user-defined materials.

[2] Chilton, Shultis, and Faw. Principles of Radiation Shielding. Prentice-Hall, Englewood Cliffs, 1984, pp. 36-43.

[3] Messenger and Ash. The Effects of Radiation on Electronic Systems. Van Nostrand Reinhold Co., New York, 1986, p. 224.

[4] van Lint, et al. Mechanisms of Radiation Effects in Electronic Materials. John Wiley and Sons, New York, 1980, p.206.

[5] Sze, S.M., ed. VLSI Technology. McGraw-Hill, New York, 1988, p. 126.

[6] Hsia and Magdo. "Radiation Damage Study of Bipolar Devices in X-Ray Lithography." Journal of Vacuum Science and Technology, B7(6), Nov/Dec 1989.

[7] Hsu, et al. "Radiation Damage and its Effect on Hot-Carrier Induced Instability of 0.5 um CMOS Devices Patterned Using Synchrotron X-Ray Lithography", The Second Workshop on Radiation-Induced and/or Process Related Electrically Active Defects in Semiconductor-Insulator Systems, MCNC, p.251.

[8] A. Vladimirescu, K. Zhang, A. R. Newton, D. O. Pederson, A. Sangiovanni-Vincentelli, SPICE Version 2G, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, August 1981.

[9] C. M. Dozier, et al., "Defect Production in SiO_2 by X-Ray and Co-60 Radiations", IEEE Trans. Nucl. Sci., Vol. NS-32, No. 6, pp. 4363-4368, December 1985.

[10] D. M. Fleetwood, et al., "Accounting for Dose-Enhancement Effects with CMOS Transistors", IEEE Trans. Nucl. Sci., Vol. NS-32, No. 6, pp. 4369-4375, December 1985.

[11] J. M. Benedetto, H. E. Boesch, Jr., and F. B. McLean, "Dose and Energy Dependence of Interface Trap Formation in Cobalt-60 and X-Ray Environments", IEEE Trans. Nucl. Sci., Vol. 35, No. 6, pp. 1260-1264, December 1988.

[12] P. S. Winokur, et, al., "Total-Dose Radiation and Annealing Studies: Implications for Hardness Assurance Testing", IEEE Trans. Nucl. Sci., Vol. NS-33, No. 6, pp. 1343-1351, December 1986.

[13] J. L. Azarewicz, "Dose Rate Effects on Total Dose Damage", IEEE Trans. Nucl. Sci., Vol. NS-33, No. 6, pp. 1420-1424, December 1986.

[14] D. Fleetwood, P. Winokur, and J. Schwank, "Using Laboratory X-ray and Cobalt-60 Irradiations to Predict CMOS Device Response in Strategic and Space Environments", IEEE Trans. Nucl. Sci., Vol. NS-35, No. 6, pp. 1497-1505, 1988.

[15] J. R. Schwank, et al., "Physical Mechanisms Contributing to Device Rebound", IEEE Trans. Nucl. Sci., Vol. NS-31, No. 6, pp. 1434-1438, December 1984.

[16] D. M. Fleetwood, P. V. Dressendorfer, and D. C. Turpin, "A Reevaluation of Worst-Case Postirradiation Response for Hardened MOS Transistors", IEEE Trans. Nucl. Sci., Vol. NS-34, No. 6, pp. 1178-1183, December 1987.

[17] T. P. Ma and P. V. Dressensorfer, ed., Ionizing Radiation Effects in MOS Devices and Circuits. John Wiley & Sons: New York, 1989.

[18] K. F. Galloway, M. Gaitan, and T. J. Russell, "A Simple Model for Separating Interface and Oxide Charge Effects in MOS Device Characteristics", IEEE Trans. Nucl. Sci., Vol. NS-31, No. 6, pp. 1497-1501, December 1984.

[19] A. G. Stanley, "Effect of Electron Irradiation on Carrier Mobilities in Inversion Layers of Insulated Gate Field Effect Transistors", IEEE Trans. Nucl. Sci., Vol. NS-14, p. 266, 1967.

[20] B. L. Bhuva, J. J. Paulos, and S. E. Diehl, "Simulation of Worst-Case Total Dose Radiation Effects in CMOS VLSI Circuits", IEEE Trans. Nucl. Sci., Vol. NS-33, No. 6, pp. 1546-1550, December 1986.

[21] R. S. Gyurcsik, D. W. Thomas, R. H. Gallimore, and B. L. Bhuva, "Timing and Area Optimization of CMOS Combinational-Logic Circuits Accounting for Total-Dose Radiation Effects", IEEE Trans. Nucl. Sci., Vol. NS-34, No. 6, pp. 1386-1391, December 1987.

[22] P. Antognetti and G. Massobrio, Semiconductor Device Modeling with SPICE. McGraw-Hill Book Co., New York, 1988, pp. 143-205.

[23] T. Meisenheimer and D. Fleetwood, "Effect of Radiation-Induced Charge on 1/f Noise in MOS Devices", IEEE Trans. Nucl. Sci., Vol. 37, No. 6, pp. 1696-1702, December 1990.

[24] N. Weste and K. Eshraghian, Principles of CMOS VLSI Design. Addison-Wesley Publishing Co., Reading, Massachusetts, 1988, p. 41.

[25] J. W. Schrankler, et al., "CMOS Scaling Implications for Total Dose Irradiation", IEEE Trans. Nucl. Sci., Vol. NS-32, No. 6, pp. 3988-3990, December 1985.

[26] Personal communication with Dr. Pradeep Bhattacharya, Associate Professor of Electrical Engineering; Louisiana State University; Baton Rouge, LA, 70803.

[27] A. Reisman, C. J. Merz, J. R. Maldonado, and W. W. Molzen, Jr., "Low Energy X-Ray and Electron Damage to IGFET Gate Insulators", J. Electrochem. Soc., Vol. 131, No. 6, pp. 1404-1409, June 1984.

[28] B. L. Henke and M. A. Tester, "Techniques of Low Energy X-Ray Spectroscopy (0.1 to 2 keV Region)", July 1974. To be published in part in Advances in X-Ray Analysis, Vol. 18, Plenum Press, 1975.

[29] Dr. Kiki Ikossi-Anastasiou, Assistant Professor of Electrical Engineering; Louisiana State University, Baton Rouge, LA, 70803. Developed a customized software package for control of the HP 4140B.

[30] N. Kaul, B. L. Bhuva, V. Rangavajjhala, H. van der Molen, and S. E. Kerns, "Simulation of Design Dependent Failure Exposure Levels for CMOS ICs", IEEE Trans. on Nucl. Sci., Vol. 37, No. 6, pp. 2097-2103, Dec. 1990.

[31] Chao-Cheng Chen, Sow-Chang Liu, Cheng-Cheng Hsiao, and Jenn-Gwo Hwu, "A Circuit Design for the Improvement of Radiation Hardness in CMOS Digital Circuits", IEEE Trans. on Nucl. Sci., Vol. 39, No. 2, pp. 272-277, April 1992.

APPENDIX A

INVERSION VOLTAGE DERIVATION

The inversion voltage for the modified inverter is derived with the assumption that N1 and P1 of Figure 5.6.1 are both in saturation and that the source of N1 is at a potential V_X. Defining the symbols used, V_X is equal to the magnitude of the NMOS threshold voltage shift ΔV_{Tn}, V_{Tno} is the initial NMOS threshold voltage, and a prime indicates use of the post-irradiation value.

$$\frac{1}{2}\beta_P(V_{DD}-V_{INV}-|V'_{Tp}|)^2 = \frac{1}{2}\beta_N(V_{INV}-V_X-V'_{Tn})^2 \qquad (A.1)$$

$$V_{DD}-V_{INV}-|V'_{Tp}| = \sqrt{\frac{\beta_N}{\beta_P}}\,(V_{INV}-V_X-V'_{Tn}) \qquad (A.2)$$

$$V_{INV}\left(1+\sqrt{\frac{\beta_N}{\beta_P}}\right) = \sqrt{\frac{\beta_N}{\beta_P}}\,(V_X+V'_{Tn})+V_{DD}-|V'_{Tp}| \qquad (A.3)$$

$$V_{INV} = \frac{V_{DD}-|V'_{Tp}|+\sqrt{\frac{\beta_N}{\beta_P}}\,(\Delta V_{Tn}+V'_{Tn})}{1+\sqrt{\frac{\beta_N}{\beta_P}}} \qquad (A.4)$$

$$V_{INV} = \frac{V_{DD}-|V'_{Tp}|+V_{Tno}\sqrt{\frac{\beta_N}{\beta_P}}}{1+\sqrt{\frac{\beta_N}{\beta_P}}} \qquad (A.5)$$

$\therefore$ V_{INV} depends on the shift in PMOS V_T, not that of the NMOS.

APPENDIX B

β_2/β_3 DERIVATION

The relationship between β_2 and β_3, N2 and N3 in Figure 5.6.1, was not directly addressed in [31]. Its derivation here assumes that N2 and N3 are in saturation since the gate voltage of N2 is $V_{OH} = V_{DD}$ when the compensation circuitry is active, and the gate voltage of N3 is slightly larger than V_{Tn} while the source of N3 is at a low potential too. This assumption is true as long as the NMOS threshold voltage is positive.

$$\frac{1}{2}\beta_2 (V_{DD}-V_{[source,N2]}-V'_{Tn})^2 = \frac{1}{2}\beta_3 (2V_g-V_{Tno}-\Delta V_{Tn})^2 \qquad (B.1)$$

$$\frac{\beta_2}{\beta_3} = \left(\frac{2V_g-V'_{Tn}}{V_{DD}-V_{[source,N2]}-V'_{Tn}}\right)^2 \qquad (B.2)$$

If β_2/β_3 is chosen to be one, the direct dependence on ΔV_{Tn} is circumvented, and the following relation results:

$$V_{[source,N2]} = V_{DD}-2V_g \ . \qquad (B.3)$$

The condition to maintain V_X at ΔV_{Tn} is therefore dependent on maintaining the source voltage of N2 at a constant value. Clearly, this is not entirely possible with the present circuit as the current through the compensation circuitry changes with dose; see Figures 5.6.3 and 5.6.5.

VITA

Roy Austin Hensley, the son of Richard and Sue Hensley, was born on March 13, 1968 in Freeport, Texas. He graduated from Angleton High School in 1986 and enrolled in the University of Texas at Austin. In 1989, he transferred to Louisiana State University at Baton Rouge and graduated with a Bachelor of Science Degree in Electrical Engineering from that institution in August 1991. He began graduate studies in Electrical Engineering at Louisiana State University in September 1991. Having completed the course requirements in December 1992, he is presently a candidate for the degree of Master of Science in Electrical Engineering.

MASTER'S EXAMINATION AND THESIS REPORT

Candidate: Roy Austin Hensley

Major Field: Electrical Engineering

Title of Thesis: Radiation Sensitivity of SPICE Model Parameters of MOSIS CMOS Devices

Approved:

A. Srivastava
Major Professor and Chairman

Daniel Fogel
Dean of the Graduate School

EXAMINING COMMITTEE:

Martin Feldman

John C Courtney

Date of Examination:

March 17, 1993